EXHIBIT A

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FAIRCHILD SEMICONDUCTOR CORP.

UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

ALPHA & OMEGA SEMICONDUCTOR, INC., a California corporation; and ALPHA & OMEGA SEMICONDUCTOR, LTD., a Bermuda corporation, Plaintiffs and Counterdefendants, v. FAIRCHILD SEMICONDUCTOR CORP., a Delaware corporation, Defendant and Counterclaimant.	Case No. C 07-2638 JSW (Consolidated with Case No. C 07-2664 JSW) **FAIRCHILD SEMICONDUCTOR CORPORATION'S DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS** **(Patent L.R. 3-1)**
AND RELATED COUNTERCLAIMS.	

Pursuant to Northern District of California Patent Local Rule 3-1, defendant and counterclaimant Fairchild Semiconductor Corporation ("Fairchild") hereby serves its Disclosure of Asserted Claims and Preliminary Infringement Contentions ("Disclosure"). This Disclosure is based on information reasonably available to Fairchild at this time. Fairchild reserves the right to supplement this Disclosure based on information developed in the course of this lawsuit through

discovery or additional factual investigation, in view of the Court's claim construction ruling or as other circumstances may require.

I. ASSERTED CLAIMS AND ACCUSED PRODUCTS

Based upon the information presently available, Fairchild contends that plaintiffs and counterdefendants Alpha & Omega Semiconductor, Inc., and Alpha & Omega Semiconductor, Ltd., (collectively, "AOS") have infringed and continue to infringe, directly and/or indirectly, the following claims of U.S. Patent Nos. 6,429,481 ("the '481 patent"), 6,521,497 ("the '497 patent"), 6,710,406 ("the '406 patent") and 6,828,195 ("the '195 patent") (collectively, "the Fairchild patents-in-suit") by making, using, offering to sell, selling within the United States, or importing into the United States the following accused products of which Fairchild is presently aware (or importing into the United States products made by methods claimed in the Fairchild patents-in-suit).

Patent Number	Asserted Claims	Accused Products
The '481 patent	Claims 1-4, 18 (against accused products with closed cell design) Claims 1-4, 6-11, 15-18, 21, 22 (against accused products with striped design)	See attached Exhibit 1
The '497 patent	Claims 1-7, 11-13, 15-17 (against accused products with closed cell design) Claims 1-9, 11-13, 15-17 (against accused products with striped design)	See attached Exhibit 1
The '406 patent	Claims 1-6, 10-12 (against accused products with closed cell design) Claims 1-6, 10-17, 24-32 (against accused products with striped design)	See attached Exhibit 1
The '195 patent	Claims 1, 2, 6-13, 21, 22 (against accused products with closed cell design) Claims 1, 2, 6-13, 15-22 (against accused products with striped design)	See attached Exhibit 1

II. CLAIM CHARTS

Claim charts identifying specifically where each element of each asserted claim is found within each accused device or the process by which each accused device was made are attached hereto as Exhibits 2 through 57. These claim charts are based on information available to Fairchild at this time and are based, in part, upon reverse engineering of a reasonable sampling of AOS products. Fairchild contends that each of the accused AOS products meets the limitations of the asserted claims because, based upon their published characteristics, they are likely to have the same design and structure as the products for which reverse engineering data is provided. In addition, each of the accused AOS products is likely to have been manufactured using a process that is the same or similar in all respects relevant to the asserted claims as the products for which reverse engineering data is provided.

To date, AOS has not provided any discovery. Additionally, prior to the commencement of this litigation, on May 17, 2007, Fairchild requested that AOS produce, subject to a confidentiality agreement, information regarding the processes by which the accused products are manufactured. AOS refused to produce the information. Consequently, Fairchild is likely to have additional evidentiary support regarding AOS's infringement after a reasonable opportunity for further investigation and discovery.

III. INFRINGEMENT

Fairchild contends that, when the terms of the asserted claims are properly construed, each limitation of each asserted claim is literally present in the corresponding accused device or in the process used to manufacture the accused device as set forth in Sections II above. In the alternative, if warranted by the Court's claim construction, Fairchild reserves the right to contend that any element not found to be literally present in an accused product is present under the doctrine of equivalents.

IV. PRIORITY DATES

Fairchild contends that the asserted claims for each of the Fairchild patents-in-suit are entitled to a priority date of November 14, 1997.

V. FAIRCHILD'S PRACTICE OF THE CLAIMED INVENTIONS

Fairchild wishes to preserve the right to rely, for any purpose, on the assertion that its own

products and/or processes practice the inventions claimed in each of the asserted claims. Accordingly, Fairchild identifies the following products and/or processes that incorporate or reflect the limitations of the corresponding asserted claims.

Patent Number	Asserted Claims	Fairchild's Products and/or Processes
6,429,481	1, 2, 3, 4, 6, 7, 8, 9, 10, 11, 15, 16, 17, 18, 21, 22	PowerTrench® MOSFETs
6,521,497		None
6,710,406	1, 2, 3, 4, 5, 6, 10, 11, 12, 13, 14, 15, 16, 17, 24, 25, 26, 27, 29, 30, 31, 32	PowerTrench® MOSFETs
6,828,195	1, 2, 6, 7, 13, 15, 16, 17, 18, 19, 20, 21, 22	PowerTrench® MOSFETs

VI. PRODUCTION OF DOCUMENTS

Fairchild produces herewith those documents within its possession, custody, or control as required by Northern District of California Patent Local Rule 3-2.

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DATED: August 31, 2007

Respectfully submitted,

By: [signature]

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FAIRCHILD SEMICONDUCTOR CORP.

61122892 v2

CERTIFICATE OF SERVICE
[C.C.P. §§ 1011 and 1013, C.R.C.§ 2008, F.R.C.P. Rule 5, F.R.A.P. 25]

I declare that I am employed in the City and County of San Francisco, California; I am over the age of 18 years and not a party to the within action; my business address is Two Embarcadero Center, Eighth Floor, San Francisco, California, 94111. On the date set forth below, I served a true and accurate copy of the document(s) entitled:

FAIRCHILD SEMICONDUCTOR CORPORATION'S DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS

on the party(ies) in this action by placing said copy(ies) in a sealed envelope each addressed as follows:

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☐ [By First Class Mail] I am readily familiar with my employer's practice for collecting and processing documents for mailing with the United States Postal Service. On the date listed herein, following ordinary business practice, I served the within document(s) at my place of business, by placing a true copy thereof, enclosed in a sealed envelope, with postage thereon fully prepaid, for collection and mailing with the United States Postal Service where it would be deposited with the United States Postal Service that same day in the ordinary course of business.

☐ [By Overnight Courier] I caused each envelope to be delivered by a commercial carrier service for overnight delivery to the offices of the addressee(s).

☒ [By Hand] I directed each envelope to the party(ies) so designated on the service list to be delivered by courier this date.

☐ [By Facsimile Transmission] I caused said document to be sent by facsimile transmission to the fax number indicated for the party(ies) listed above.

☐ [By Electronic Transmission] I caused said document to be sent by electronic transmission to the e-mail address(es) indicated for the party(ies) listed above.

I declare under penalty of perjury that the foregoing is true and correct and that this declaration was executed this date at San Francisco, California.

Dated: August 31, 2007.

Scott Wortman

61122892 v2

EXHIBIT 1

ALPHA & OMEGA SEMICONDUCTOR

MOSFET Selector Guide - All Products

Part Number	Status	Replacement Part	Package	Configuration	Popular Application	Type	ESD Diode	Schottky Diode	Schottky Type	V_{DS} (V)	V_{GS} (±V)	I_D (A) 25°C	I_D (A) 70°C	P_D (W) 25°C	P_D (W) 70°C	$R_{DS(ON)}$ (mΩ max) at V_{GS}* 10V	4.5V	2.5V	1.8V	VGS(th) (max V)	Ciss (pF)	Crss (pF)	Qg (nC)	Qgd (nC)	Td(on) (ns)	Td(off) (ns)
						P	No	No		-30	25	-8	-6.9	2	1.44	19				-3	2076	302	*39	11.4	12.7	25.2
AO4604	Not for new designs	AO4619	SO-8	Complementary	Inverter	N	No	No		30	20	6.8	5.8	2	1.44	28	42			3	680	77	6.74	3.2	4.6	20.6
						P	No	No		-30	20	-5	-4.2	2	1.44	52	87			-3	700	75	7.6	3.8	6.3	29
AO4606	Not for new designs	AO4620	SO-8	Complementary	Inverter	N	No	No		30	20	8.9	5.8	2	1.44	28	42			3	680	77	6.74	3.2	4.6	20.6
						P	No	No		-30	20	-6	-5	2	1.44	35	58			-2.4	920	122	9.6	4.5	7.7	20.2
AO4607	Full Production		SO-8	Complementary	Inverter	N	No	Yes	1A	30	20	6.9	5.8	2	1.28	28	42			3	680	77	6.74	3.2	4.6	20.6
						P	No	No		-30	20	-6	-5	2	1.28	35	58			-2.4	920	122	9.6	4.5	7.7	20.2
AO4609	Not for new designs	AO4622	SO-8	Complementary	Inverter	N	No	No		30	20	8.5	6.6	2	1.28	18	28			3	1040	110	9.36	4.2	5.2	17.3
						P	No	No		-30	12	-3	-2.4	2	1.28	130	180	260		-1.4	409	42	4.4	1.32	5.3	31.5
AO4611	Full Production		SO-8	Complementary	Inverter	N	No	No		60	20	6.3	5	2	1.28	25	30			3	1920	116	24.2	14.4	7.6	28.9
						P	No	No		-60	20	-4.8	-3.9	2	1.28	42	52			-3	2417	120	22.8	9.6	9.8	44
AO4612	Full Production		SO-8	Complementary	Inverter	N	No	No		60	20	4.5	3.6	2	1.28	56	77			3	450	25	4.3	2.2	4.7	15.7
						P	No	No		-60	20	-3.2	-2.6	2	1.28	105	135			-3	930	35	8	3.2	8	31.5
AO4613	Full Production		SO-8	Complementary	Inverter	N	Yes	No		30	20	7.2	6.1	2	1.44	24	40			3	522	75	5.3	4	4.7	16.2
						P	Yes	No		-30	20	-6.1	-5.1	2	1.44	37	60			-3	1040	134	8.7	5	9	22.7
AO4614	Not for new designs	AO4614A	SO-8	Complementary	Inverter	N	No	No		40	20	6	5	2	1.28	31	45			3	404	37	4.2	2.3	4.2	15.6
						P	No	No		-40	20	-5	-4	2	1.28	45	63			-3	657	63	8.8	3.9	7.5	26
AO4614A	New		SO-8	Complementary	Inverter	N	No	No		40	20	6	5	2	1.28	31	45			3	404	37	4.2	2.3	4.2	15.6
						P	No	No		-40	20	-5	-4	2	1.28	45	63			-3	657	63	6.8	3.9	7.5	26
AO4615	Full Production		SO-8	Complementary	Inverter	N	Yes	No		30	20	7.2	6.1	2	1.44	24	40			3	522	75	5.3	4	4.7	16.2
						P	es + 1M	No		-30	20	-5.7	-4.9	2	1.44	39	62			-3	1035	99	8.9	4.1	8	19.5
AO4616	Full Production		SO-8	Complementary	Inverter	N	No	No		30	20	8.5	6.5	2	1.28	20	28			3	1040	110	9.36	4.2	5.2	17.3
						P	No	No		-30	20	-7.1	-5.6	2	1.28	25	40			-2.7	1573	211	16.1	4.4	9.5	44.2
AO4617	Full Production		SO-8	Complementary	Inverter	N	Yes	No		40	20	6	5	2	1.28	32	45			3	506	38	4.1	2.7	4.8	17
						P	Yes	No		-40	20	-5	-4	2	1.28	48	75			-3	1006	77	8.9	4.6	9.7	35.5
AO4619	New		SO-8	Complementary	Inverter	N	No	No		30	20	7.4	6	2	1.3	24	36			3	621	85	5.7	3	4.5	15.1
						P	No	No		-30	20	-5.2	-4.2	2	1.3	48	74			-3	680	86	6.4	4	7.7	20
AO4627	New		SO-8	Complementary	Inverter	N	No	No		30	20	7.2	6.2	2	1.44	24	36			3	660	87	5.7	3	4.5	15.1
						P	No	No		-30	20	-5.3	-4.5	2	1.44	38	60			-3	980	115	9.8	4.8	7.7	20
AO4622	New		SO-8	Complementary	Inverter	N	No	No		20	18	7.3	6.2	2	1.44	23	30	84		2	900	105	7.2	2.8	4.5	18.7
						P	No	No		-20	12	-5	-4.2	2	1.44		53	87		-1.3	800	103	7.4	2.9	4.4	44
AO4624	New		SO-8	Complementary	Inverter	N	No	No		30	20	6.9	5.8	2	1.44	28	42			3	737	73	6.74	3.2	4.6	20.6
						P	No	No		-30	20	-6	-5	2	1.44	35	58			-2.4	920	122	9.6	4.5	7.7	20.2
AO4701	Full Production		SO-8	Single	SMPS Low Side	P	No	Yes	3A	-30	12	-5	-4.2	2	1.44	49	64	120		-1.3	952	77	9.5	3.1	12	37
AO4702	Not for new designs	AO4712	SO-8	Single	SMPS Low Side	N	No	Yes	1A	30	20	11	9.3	3	2	16	25			3	1040	121	9.8	3.5	4.5	17.4
AO4704	Not for new designs	AO4710	SO-8	Single	SMPS Low Side	N	No	Yes	1A	30	12	13	10.4	3.1	2	11.5	13			2	3656	168	30.5	8.6	6.2	55
AO4706	New		SO-8	Single	SMPS Low Side	N	No	Yes	SRFET	30	12	16.5	13.2	3.1	2	6.8	8.2			2.4	4000	217	27	11	9	37
AO4708	New		SO-8	Single	SMPS Low Side	N	No	Yes	SRFET	30	12	15	12	3.1	2	8.7	10.5			2.4	2800	145	19	6	7	31
AO4710	New		SO-8	Single	SMPS Low Side	N	No	Yes	SRFET	30	12	12.7	10	3.1	2	11.8	14.2			2.3	1980	111	15	6	5.5	27
AO4712	New		SO-8	Single	SMPS Low Side	N	No	Yes	SRFET	30	12	11.2	9.1	3.1	2	14.5	18			2.4	1450	92	12	4.2	5.5	24
AO4714	New		SO-8	Single	SMPS Low Side	N	No	Yes	SRFET	30	20	20	16	3	2	4.7	6.7			2.2	3760	314	29	12	9.5	34
AO4716	New		SO-8	Single	SMPS Low Side	N	No	Yes	SRFET	30	20	16.5	13	3.1	2	7	10			2	2154	185	17.8	7.6	6.8	25.2
AO4718	New		SO-6	Single	SMPS Low Side	N	No	Yes	SRFET	30	20	15	12	3.1	2	9	14			2.5	1620	162	12	5.6	6.3	21.6
AO4720	New		SO-8	Single	SMPS Low Side	N	No	Yes	SRFET	30	20	13	10.5	3.1	2	11	17.5			2	1267	118	10.4	3.6	5.2	21.2
AO4722	New		SO-8	Single	SMPS Low Side	N	No	Yes	SRFET	30	20	11.6	9.3	3.1	2	14	22			2.5	903	91	7.8	3.9	5	17.8
AO4724	New		SO-8	Single	SMPS Low Side	N	No	Yes	SRFET	30	20	10.5	8.5	3.1	2	17.5	28			2	696	81	6.1	2.7	2.6	17
AO4800	Not for new designs	AO4800B	SO-8	Dual	General Purpose	N	No	No		30	12	6.9	5.8	2	1.44	27	32	50		1.4	858	80	9.6	3	3.2	26.3
AO4800B	New		SO-8	Dual	General Purpose	N	No	No		30	12	6.9	5.8	1.9	1.2	27	32	50		1.5	900	65	10	3.75	3.2	21.5
AO4801	Not for new designs	AO4801A	SO-8	Dual	General Purpose	P	No	No		-30	12	-5	-4.2	2	1.44	49	64	120		-1.3	952	77	9.5	3.1	12	37
AO4801A	New		SO-8	Dual	General Purpose	P	No	No		-30	12	-5.6	-4.5	2	1.3	42	52	75		-1.3	933	81	9.3	3.7	5.2	42
AO4803	Not for new designs	AO4803A	SO-8	Dual	General Purpose	P	No	No		-30	20	-5	-4.2	2	1.4	52	87			-3	700	75	14.7	3.8	8.3	29
AO4803A	New		SO-8	Dual	General Purpose	P	No	No		-30	20	-5	-4	2	1.3	46	74			-2.5	668	92	6.4	4	7.7	20
AO4805	Full Production	AO4817	SO-8	Dual	Load Switch	P	No	No		-30	25	-8	-6.9	2	1.44	18				-3	2076	302	*39	11.4	12.7	25.2
AO4806	Full Production	AO4806A	SO-8	Dual	General Purpose	N	Yes	No		20	12	9.4	7.5	2	1.28	14	16	22	30	1	1810	200	17.9	4.7	3.3	44
AO4807	Full Production		SO-8	Dual	General Purpose	P	No	No		-30	20	-6	-5	2	1.44	35	58			-2.4	920	122	8.8	4.5	7.7	20.2
AO4812	Not for new designs	AO4842	SO-8	Dual	General Purpose	N	No	No		30	20	6.9	5.8	2	1.44	28	42			3	680	77	6.74	3.2	4.6	20.6
AO4813	Full Production		SO-8	Dual	General Purpose	P	No	No		-30	20	-7.1	-5.6	2	1.28	25	40			-2.7	1573	211	16.1	4.4	9.5	44.2
AO4815	Full Production		SO-6	Dual	Load Switch	P	Yes	No		-30	25	-8	-6.9	2	1.44	20				-3	2330	320	*41	12	13	51
AO4817	Full Production		SO-8	Dual	Load Switch	P	Yes	No		-30	25	-8	-6.9	2	1.44	21				-3	1760	255	*30	8	12.5	40
AO4818	Not for new designs	AO4818B	SO-8	Dual	General Purpose	N	No	No		30	20	8.5	6.6	2	1.28	19	28			3	1040	110	9.36	4.2	5.2	17.3
AO4818B	New		SO-8	Dual	General Purpose	N	No	No		30	20	8.5	6.6	2	1.28	16	26			3	955	112	9	4.7	5	19
AO4821	Full Production		SO-8	Dual	Load Switch	P	Yes	No		-12	8	-8	-6.7	2	1.28		18	22	29	-1	3960	757	37	11	15	158
AO4822	Not for new designs	AO4822A	SO-8	Dual	General Purpose	N	No	No		30	20	8.5	6.6	2	1.28	16	28			3	1040	110	9.36	4.2	5.2	17.3
AO4822A	New		SO-8	Dual	General Purpose	N	No	No		30	20	8.5	6.6	2	1.28	16	26			3	955	112	9	4.7	5	19
AO4824	Not for new designs	AO4924	SO-8	Asymmetric	SMPS	N	No	No		30	20	8.5	6.8	2	1.28	17	27			3	1040	110	8.36	4.2	5.2	17.3
						N	No	No		30	12	9.8	7.8	2	1.28	13	15			2	3656	188	30.5	8.5	6.5	52.4
AO4826	Full Production		SO-8	Dual	General Purpose	N	No	No		60	20	6.3	5	2	1.28	25	30			3	1920	116	24.2	14.4	7.8	28.9
AO4828	Full Production		SO-8	Dual	General Purpose	N	No	No		60	20	4.5	3.6	2	1.28	56	77			3	450	25	4.3	2.2	4.7	15.7
AO4840	Full Production		SO-8	Dual	General Purpose	N	Yes	No		40	20	6	5	2	1.28	31	45			3	404	37	4.2	2.3	4.2	15.6
AO4842	Full Production		SO-8	Dual	General Purpose	N	Yes	No		30	20	7.5	6.4	2	1.44	22	35			3	621	85	6	3	4.5	15.1
AO4850	New		SO-8	Dual	Inverter	N	No	No		75	25	3.1	2.4	2	1.3	130	165			3	290	24	*5.14	1.18	4	14.4
AO4900	Not for new designs	AO4924	SO-8	Dual	SMPS	N	No	Yes	1A	30	12	6.9	5.8	2	1.44	27	32	50		1.4	846	67	9.6	3	3.2	26.3
AO4906	Not for new designs	AO4932	SO-8	Dual	SMPS	N	No	Yes	1A	30	12	7	6	2	1.44	27	32	50		1.4	846	67	9.6	3	3.2	26.3
AO4912	Not for new designs	AO4932	SO-8	Asymmetric	SMPS	N	No	Yes		30	12	7	6.4	2	1.28	26	31			2	590	40	6.04	2.56	3.7	14.9
						N	No	Yes	1A	30	20	8.5	6.8	2	1.28	17	25			3	970	110	9.36	4.2	5.2	17.3
AO4914	Not for new designs	AO4924	SO-8	Dual	SMPS	N	No	Yes	1A	30	20	8.5	6.6	2	1.28	18	28			3	971	110	9.36	4.2	5.2	17.3
AO491[illegible]	[illegible]t for new designs	AO4932	SO-8	Dual	SMPS	N	No	Yes	1A	[illegible]	20	8.5	6.6	2	1.28	17	27			3	971	110	9.36	4.2	5	17.3

* Qg measured with Vgs = 10V. In all other cases Vgs = 4.5V.

EXHIBIT 1

ALPHA & OMEGA SEMICONDUCTOR

MOSFET Selector Guide - All Products

Part Number	Status	Replacement Part	Package	Configuration	Popular Application	Type	ESD Diode	Schottky Diode	Schottky Type	V_{DS} (V)	V_{GS} (±V)	I_D (A) 25°C	I_D (A) 70°C	P_D (W) 25°C	P_D (W) 70°C	$R_{DS(ON)}$ (mΩ max) at V_{GS}* 10V	4.5V	2.5V	1.8V	VGS(th) (max V)	Ciss (pF)	Crss (pF)	Qg (nC)	Qgd (nC)	Td(on) (ns)	Td(off) (ns)
AO4918	New		SO-8	Asymmetric	SMPS	N	No			30	20	8.3	6.7	2	1.28	18	27			3	1040	110	9.36	4.2	5.2	17.3
						N	No	Yes	SRFET	30	12	9.3	7.4	2	1.28	14.5	18			2	3740	186	30.5	8.5	6	54.5
AO4922	New		SO-8	Asymmetric	SMPS	N	No			30	12	7.3	5.9	2	1.3	24	29	48		1.5	900	65	10	3.75	3.2	21.5
						N	No	Yes	SRFET	30	12	9	7.2	2	1.3	15.8	18.5			2.4	1980	111	15	6	5.5	27
AO4924	New		SO-8	Asymmetric	SMPS	N	No			30	12	7.3	5.9	2	1.3	24	29			1.5	800	65	10	3.75	3.2	21.5
						N	No	Yes	SRFET	30	12	9	7.2	2	1.3	15.8	19.5			2.4	1450	82	12	4.2	5.5	24
AO4926	New		SO-8	Asymmetric	SMPS	N	No			30	12	7.3	5.9	2	1.3	24	29	48		1.5	900	65	10	3.75	3.2	21.5
						N	No	Yes	SRFET	30	12	9.5	7.8	2	1.3	13.6	16			2.4	1980	111	15	6	5.5	27
AO4928	New		SO-8	Asymmetric	SMPS	N	No			30	12	7.3	5.8	2	1.3	24	29	48		1.5	900	65	10	3.75	3.2	21.5
						N	No	Yes	SRFET	30	12	9	7.2	2	1.3	16	19.5			2.4	1450	92	12	4.2	5.5	24
AO4930	New		SO-8	Asymmetric	SMPS	N	No			30	20	8	7.2	2	1.3	15.8	23			2.3	955	112	9	4.7	5	19
						N	Nu	Yes	SRFET	30	12	9.5	7.6	2	1.3	13.5	16			2.4	1980	111	15	6	5.5	27
AO4932	New		SO-8	Asymmetric	SMPS	N	No			30	20	9	7.2	2	1.3	15.8	23			2.3	955	112	9	4.7	5	19
						N	No	Yes	SRFET	30	12	9	7.2	2	1.3	15.8	19.6			2.4	1450	92	12	4.2	5.5	24
AO4936	New		SO-8	Asymmetric	SMPS	N	No			30	20	8.5	6.8	2	1.3	18	28			2.3	955	112	9	4.7	5	19
						N	No	Yes	SRFET	30	20	8.8	7.1	2	1.3	16	22			2	1267	118	10.4	3.6	5.2	21.2
AO4938	New		SO-8	Asymmetric	SMPS	N	No			30	20	9	7.2	2	1.3	16	26			2.3	955	112	9	4.7	5	19
						N	No	Yes	SRFET	30	20	9.6	7.7	2	1.3	13.5	19.5			2	1267	118	10.4	3.6	5.2	21.2
AO4940	New		SO-9	Asymmetric	SMPS	N	No			30	20	7.5	6	2	1.3	23	36			2.5	821	85	5.7	3	4.5	15.1
						N	No	Yes	SRFET	30	20	9.1	7.3	2	1.3	15	23			2.5	903	91	7.8	3.9	5	17.8
AO4944	New		SO-8	Dual	SMPS	N	No	Yes		30	12	8.6	6.9	2	1.3	16	20			2.4	1450	92	12	4.2	5.5	24
AO4946	New		SO-8	Dual	SMPS	N	No	Yes		30	12	8.6	6.9	2	1.3	16	20			2.4	1450	92	12	4.2	5.5	24
AO4948	New		SO-8	Asymmetric	SMPS	N	No			30	20	8.5	6.8	2	1.3	18	28			2.3	955	112	9	4.7	5	19
						N	No	Yes	SRFET	30	20	8.8	7.1	2	1.3	16	22			2	1267	118	10.4	3.6	5.2	21.2
AO5800	New		SC89-6	Dual	Load Switch	P	Yes	No		60	20	0.4	0.3	0.4	0.24	1600	1900			2.5	41	6	1		39.2	261
AO5803	New		SC89-6	Dual	Load Switch	P	Yes	No		-20	8	-0.6	-0.4	0.4	0.24		800	1000	1250	-0.9	72	9	0.6		80.5	612
AO6400	Full Production		TSOP-6	Single	General Purpose	N	No	No		30	12	6.8	5.8	2	1.44	28	33	52		1.4	823	77	9.6	3	5.5	37
AO6401	Full Production	AO6401A	TSOP-6	Single	General Purpose	P	No	No		-30	12	-5	-4.2	2	1.44	49	64	119		-1.3	943	73	9.5	2.9	6	40
AO6402	Not for new designs	AO6402A	TSOP-6	Single	General Purpose	N	No	No		30	20	6.9	5.8	2	1.44	28	42			3	660	77	6.74	3.2	4.6	20.6
AO6402A	New		TSOP-6	Single	General Purpose	N	No	No		30	20	7	5.6	2	1.28	27	40			2.5	821	85	5.7	3	4.5	15.1
AO6403	Full Production		TSOP-6	Single	General Purpose	P	No	No		-30	20	-6	-5	2	1.44	35	58			-2.4	920	122	9.6	4.5	7.7	20.2
AO6404	Full Production		TSOP-6	Single	Load Switch	N	No	No		20	12	8.6	6.8	2	1.28	17	18	24	33	1	1810	200	17.9	4.7	2.5	49
AO6405	Full Production		TSOP-6	Single	General Purpose	P	No	No		-30	20	-5	-4.2	2	1.4	52	87			-3	700	75	7.6	3.8	8.3	29
AO6408	Full Production		TSOP-6	Single	General Purpose	N	Yes	No		20	12	8.8	7	2	1.28	18	20	25	32	1	1810	200	17.9	4.7	3.3	44
AO6409	Full Production		TSOP-6	Single	Load Switch	P	Yes	No		-20	8	-5	-4.2	2	1.28		45	56	75	-1	1450	160	17.2	4.5	9	91
AO6414	Full Production		TSOP-6	Single	General Purpose	N	No	No		55	12	2.3	1.9	1.56	1.1		160	200		2	214	12.6	2.6	0.8	2.3	16.5
AO6415	Full Production		TSOP-6	Single	Load Switch	P	Yes	No		-20	12	-3.3	-2.7	1.25	0.8	75	100	150		-1.4	512	62	4.9	1.2	11	34
AO6420	Full Production		TSOP-6	Single	General Purpose	N	No	No		60	20	4.2	3.4	2	1.28	60	75			3	450	25	4.3	2.2	5.1	15.8
AO6601	Full Production		TSOP-6	Complementary	Inverter	N	No	No		30	12	3.4	2.7	1.15	0.73	60	75	115		1.4	390	41	4.34	0.6	4	22
						P	No	No		-30	12	-2.3	-1.8	1.15	0.73	135	185	285		-1.4	409	42	4.8	0.72	13	28
AO6602	Full Production		TSOP-6	Complementary	Inverter	N	No	No		30	20	3.1	2.4	1.15	0.73	75	115			3	200	20	3.1	1.6	3.3	13.2
						P	No	No		-30	20	-2.7	-2.1	1.15	0.73	100	160			-3	260	44	3	1.8	7	15
AO6604	Full Production		TSOP-6	Complementary	Inverter	N	No	No		20	8	3.4	2.7	1.15	0.73		60	75	100	1	436	44	6.2	0.5	5.5	40
						P	No	No		-20	8	-2.5	-2	1.15	0.73		110	140	200	-1	540	49	6.1	1.6	10	44
AO6605	Full Production		TSOP-6	Complementary	Load Switch	N	No	No		20	8	1.7	1.4	1.15	0.73		200	270	400	0.8	101	14	1.6	0.4	3.2	15.5
						P	No	No		-20	8	-2.5	-2	1.15	0.73		97	130	190	-1	540	49	6.1	1.6	12	49
AO6700	Full Production		TSOP-6	Single	SMPS	N	No	Yes	1A	20	8	4.1	3.3	1.39	0.89		50	65	95	1	449	51.6	5.9	1.3	4.5	32.7
AO6701	Full Production		TSOP-6	Single	SMPS	P	Nu	Yes	1A	-30	12	-2.3	-1.8	1.15	0.7	135	185	265		-1.4	409	42	4.9	1.6	6.9	38.5
AO6702	Full Production		TSOP-6	Single	SMPS	N	No	Yes	1A	20	8	3.8	3	1.15	0.7		50	65	95	1	449	51.6	5.9	1.3	4.5	32.7
AO6704	Full Production		TSOP-6	Single	SMPS	N	No	Yes	1A	30	12	3.6	2.9	1.39	0.89	65	75	160		1.8	226	29	3	0.55	2.6	14.5
AO6706	Full Production		TSOP-6	Single	SMPS	N	No	Yes	1A	30	12	3.3	2.6	1.15	0.7	65	75	180		1.8	226	29	3	0.55	2.8	14.5
AO6800	Full Production		TSOP-6	Dual	General Purpose	N	No	No		30	12	3.4	2.7	1.15	0.73	60	75	115		1.4	390	41	4.96	1.72	6.8	35.2
AO6801	Full Production		TSOP-6	Dual	General Purpose	P	No	No		-30	12	-2.3	-1.8	1.15	0.73	135	185	265		-1.4	409	42	4.9	1.6	6.9	38.5
AO6802	Full Production		TSOP-6	Dual	General Purpose	N	No	No		30	20	3.1	2.4	1.15	0.73	75	115			3	200	20	3.1	1.6	3.3	13.2
AO7400	Full Production		SC70-3	Single	General Purpose	N	No	No		30	12	1.7	1.3	0.35	0.22	85	100	140		1.4	390	41	4.82	1.58	2.5	22
AO7401	Full Production		SC70-3	Single	General Purpose	P	No	No		-30	12	-1.2	-1	0.35	0.22	150	200	280		-1.4	409	42	5.06	1.58	6.2	41.2
AO7402	Full Production		SC70-3	Single	General Purpose	N	No	No		20	8	1.6	1.2	0.35	0.22		90	105	130	0.9	458	54	6.05	1.45	7.3	40
AO7403	Full Production		SC70-3	Single	General Purpose	P	Yes	No		-20	8	-0.7	-0.5	0.35	0.22		470	625	800	-0.9	114	14	1.44	0.35	8.5	18.2
AO7404	Full Production		SC70-3	Single	General Purpose	N	Yes	No		20	8	1	0.75	0.35	0.22		225	290	425	0.8	101	14	1.57	0.36	3.2	15.5
AO7405	Full Production		SC70-6	Single	General Purpose	P	No	No		-30	12	-1.6	-1.3	0.625	0.4	150	200	280		-1.4	408	42	5.06	1.58	6.2	41.2
AO7407	Full Production		SC70-3	Single	General Purpose	P	No	No		-20	8	-1.2	-1	0.35	0.22		135	170	220	-1	540	49	6.2	1.44	12	74
AO7408	Full Production		SC70-6	Single	General Purpose	N	No	No		20	8	2.2	1.75	0.625	0.4		70	85	110	0.8	458	54	6.05	1.45	7.3	40
AO7410	Full Production		SC70-3	Single	General Purpose	N	No	No		30	12	1.6	1.3	0.35	0.22	90	100	175		1.6	226	29	3	1.2	2.8	17.4
AO7411	Full Production		SC70-6	Single	General Purpose	P	No	No		-20	8	-1.8	-1.5	0.625	0.4		120	150	200	-0.6	524	73	6.24	1.84	10.5	54.5
AO7412	Full Production		SC70-6	Single	General Purpose	N	No	No		30	12	2.1	1.7	0.625	0.4	80	100	180		1.8	228	29	3	1.2	2.8	17.4
AO7413	Full Production		SC70-3	Single	General Purpose	P	Yes	No		-20	12	-1.4	-1.2	0.35	0.22	113	135	180		-1.4	512	82	4.9	3.7	11	34
AO7415	Full Production		SC70-6	Single	General Purpose	P	Yes	No		-20	12	-2	-1.6	0.625	0.4	100	125	170		-1.4	512	62	4.9	3.7	11	34
AO7600	Full Production		SC70-6	Complementary	Inverter	N	No	No		20	8	0.9	0.7	0.3	0.19		300	350	450	0.9	101	14	1.57	0.36	3.2	15.5
						P	No	No		-20	8	-0.6	-0.48	0.3	0.19		550	700	950	-0.9	114	14	1.44	0.35	6.5	18.2
AO7800	Full Production		SC70-6	Dual	General Purpose	N	Yes	No		20	8	0.9	0.7	0.3	0.19		235	310	415	0.8	101	14	1.57	0.36	3.2	15.5
AO7801	Full Production		SC70-6	Dual	General Purpose	P	No	No		-20	8	-0.6	-0.48	0.3	0.19		520	700	950	-0.9	114	14	1.44	0.35	6.5	18.2
AO8403	Full Production		TSSOP-8	Single	Load Switch	P	Yes	No		-20	8	-4	-3.5	1.5	1		42	52	70	-1	954	77	9.4	3	6.3	38.2
AO8701	Full Production		TSSOP-8	Single	Load Switch	P	No	Yes	1A	-30	12	-4.2	-3.5	1.4	1	50	85	120		-1.3	1450	160	17.2	4.5	9.5	94
AO8801	Full Production		TSSOP-8	Dual	Load Switch	P	Yes	No		-20	8	-4.7	-3.7	1.4	0.9		42	53	70	-1	1450	160	17.2	4.5	9.5	94
AO8803	Full Production		TSSOP-8	Dual	Load Switch	P	Yes	No		-12	8	-7	-5.6	1.4	0.9		18	22	29	-1	3960	757	36.6	10	[illegible]	158

* Qg measured with Vgs = 10V. In all other cases Vgs = 4.5V.

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Part Number	Status	Replacement Part	Package	Configuration	Popular Application	Type	ESD Diode	Schottky Diode	Schottky Type	V_{DS} (V)	V_{GS} (±V)	I_D (A)		P_D (W)		$R_{DS(on)}$ (mΩ max) at V_{GS}*				VGS(th) (max V)	Ciss (pF)	Crss (pF)	Qg (nC)	Qgd (nC)	Td(on) (ns)	Td(off) (ns)
												25°C	70°C	25°C	70°C	10V	4.5V	2.5V	1.8V							
AO8804	Not for new designs		TSSOP-8	Common Drain	Battery Protection	N	Yes	No		20	12	8	6.3	1.5	1.08	13	14	19	27	1	1810	200	18.6	5	3.3	44
AO8806	Last Time Buy		TSSOP-8	Common Drain	Battery Protection	N	Yes	No		20	8	6.4	5.4	1.5	1.08		25	30	40	1	940	133	15	4	6.5	56.5
AO8808A	Full Production		TSSOP-8	Dual	Battery Protection	N	Yes	No		20	12	8	6.3	1.4	1	14	15	20	28	1	1180	146	16	3.8	6.2	51.7
AO8810	Full Production		TSSOP-8	Common Drain	Battery Protection	N	Yes	No		20	8	7	5.7	1.5	1		20	24	32	1	1810	200	17.9	4.7	2.5	49
AO8814	Not for new designs		TSSOP-8	Common Drain	Battery Protection	N	Yes	No		20	12	7.5	6	1.5	0.86	16	18	24	34	1	1390	150	15.4	4	6.2	40.5
AO8816	Not for new designs		TSSOP-8	Common Drain	Battery Protection	N	No	No		30	12	8	8	1.5	1	15	17	23		1.4	800	120	12	3	7	29
AO8818	Not for new designs		TSSOP-8	Common Drain	Battery Protection	N	Yes	No		30	12	7	5.5	1.5	0.96	18	20	27		1	630	137	9.3	3.6	5.7	31.5
AO8820	Full Production		TSSOP-8	Common Drain	Battery Protection	N	Yes	No		20	12	7	5.5	1.5	0.96	21	24	32	50	1	1130	125	14	5.5	5.7	36
AO8822	Full Production		TSSOP-8	Common Drain	Battery Protection	N	No	No		20	12	7	5.7	1.5	0.96	21	24	32	50	1	1060	90	14	4.6	8.7	36
AO8830	New		TSSOP-8	Common Drain	Battery Protection	N	Yes	No		20	12	6	4.8	1.5	0.94	27	30	41	55	1	290	40	5.2	1.9	280	2350
AO8842	New		TSSOP-8	Common Drain	Battery Protection	N	Yes	No		20	12	7	5.5	1.5	0.96	19.5	21	28.5	43	1	1026	157	12.4	3.5	0.96	7
AO9926B	Full Production		SO-8	Dual	Battery Protection	N	No	No		20	12	7.6	6.1	2	1.8	23	26	34	52	1	630	137	8.8	3.7	5.5	29
AOB403	Obsolete		TO-263	Single	Inverter	P	No	No		-60	20	-30	-20	83	42	44	55			-3	2977	153	20.8	10	13.7	37
AOB405	Obsolete		TO-263	Single	Inverter	P	No	No		-40	20	-12	-12	50	25	48	72			-3	657	63	7	4.1	8	24
AOB414	Obsolete		TO-263	Single	SMPS Low Side	N	No	No		30	12	110	80	100	50	4.2	4.8			1.5	9130	387	72.4	18.4	15	106.5
AOB416	Obsolete		TO-263	Single	SMPS Low Side	N	No	No		30	20	110	78	100	50	4.5	6.5			2.4	6060	355	46.4	16	15.5	52.5
AOB418	Obsolete		TO-263	Single	SMPS High Side	N	No	No		30	12	110	88	100	50	6	7.2			2	2100	165	18.6	8	5.9	34
AOB420	Obsolete		TO-263	Single	SMPS High Side	N	No	No		30	20	110	65	100	50	8.5	10			2.5	1320	154	13.3	6.7	7.7	22.2
AOB428	Obsolete		TO-263	Single	General Purpose	N	No	No		105	25	40	28	100	50	28				4	2038	85	*38.5	13.4	12.7	31.5
AOB430	Obsolete		TO-263	Single	General Purpose	N	No	No		60	20	12	12	50	26	83	85			3	450	27	3.8	1.9	4.2	16
AOB432	Obsolete		TO-263	Single	General Purpose	N	No	No		40	20	12	11	47	23	32	50			3	404	37	4.5	2.8	4	12
AOB434	Obsolete		TO-263	Single	SMPS High Side	N	No	No		25	20	55	55	50	25	9.5	15			3	1230	190	12.7	7.4	6.5	18
AOB436	Obsolete		TO-263	Single	SMPS Low Side	N	No	No		25	20	55	55	50	25	7	11			3	1850	275	16.8	8.5	7.5	25
AOD400	Not for new designs	AOD476	TO-252	Single	SMPS	N	No	Nd		30	12	10	10	20	10	30	36	52		1.4	857	71	8.7	3.1	3.5	25
AOD402	Not for new designs	AOD476	TO-252	Single	SMPS	N	No	No		30	25	18	12	60	30	18	44			3	769	131	*15.8	4.92	6.2	16
AOD403	Full Production		TO-252	Single	Load Switch	P	No	No		-30	25	-65	-65	100	50	7.6				-3.5	4360	762	*93.2	29.2	18	51
AOD404	Not for new designs	AOD494	TO-252	Single	SMPS High Side	N	No	No		30	12	85	85	100	50	7	8			2	2100	165	19.7	7.9	5.9	36.2
AOD405	Last Time Buy 6/1/07		TO-252	Single	General Purpose	P	No	No		-30	20	-18	-18	60	30	32	60			-2.4	920	122	9.7	5.4	9	20
AOD406	Not for new designs	AOD4132	TO-252	Single	SMPS Low Side	N	No	Nd		30	12	85	75	100	50	5	5.7			1.5	9130	387	72.4	16.8	14.7	105.5
AOD407	Full Production		TO-252	Single	General Purpose	P	No	No		-60	20	-12	-10	50	25	115	150			-3	987	48	7.4	3.5	9	25
AOD408	Last Time Buy 6/1/07		TO-252	Single	SMPS	N	No	No		30	20	18	18	60	30	18	27			2.5	1040	110	9.8	3.5	4.5	17.4
AOD409	Full Production		TO-252	Single	General Purpose	P	No	No		-60	20	-26	-18	60	30	40	55			-2.4	2977	153	22.2	10	12	38
AOD410	Not for new designs		TO-252	Single	General Purpose	N	No	No		30	20	8	6	25	12.5	65	105			3	288	38	3.34	1.78	3.7	15.6
AOD4100	Full Production		TO-252	Single	SMPS High Side	N	No	No		25	30	50	29	50	25	12				4	1100	200	*17	6.8	9.5	11.5
AOD4102	Full Production		TO-252	Single	SMPS	N	No	No		30	20	12	12	21	10	37	64			3	360	30	3.2	2.2	4.3	12.8
AOD4104	Full Production		TO-252	Single	SMPS Low Side	N	No	No		25	30	75	75	100	50	5.4				4	2100	400	*40	14	12	15
AOD4106	Full Production		TO-252	Single	SMPS Low Side	N	No	No		25	30	50	50	75	38	8.1				4	1561	323	*22.5	10	12	17
AOD4110	Full Production		TO-252	Single	SMPS Low Side	N	No	No	SRFE7	30	20	40	40	63	31	7.2	10.5			2	2154	185	17.8	7.6	6.8	25.2
AOD4112	Full Production		TO-252	Single	SMPS Low Side	N	No	No	SRFET	30	20	20	20	50	25	9.5	14.5			2.5	1620	162	12	5.6	6.3	21.6
AOD4120	Full Production		TO-252	Single	SMPS	N	No	No		20	16	25	23	33.3	16.7	18	25	75		2	900	105	7.2	2.8	4.5	18.7
AOD413	Full Production		TO-252	Single	General Purpose	P	No	No		-40	20	-12	-12	50	25	45	69			-3	652	63	7	4.1	8	24
AOD4132	Full Production		TO-252	Single	SMPS Low Side	N	No	Nu		30	20	85	63	100	50	4	6			3	3700	390	33	17.8	12	40
AOD414	Not for new designs	AOD472	TO-252	Single	SMPS Low Side	N	No	No		30	20	85	73	100	50	5.2	7			2.4	6060	355	46.4	15.6	15.7	55.5
AOD417	Full Production		TO-252	Single	Inverter	P	No	No		-30	20	-25	-20	50	25	34	55			-3	920	90	8.2	3.6	8	22
AOD420	Last Time Buy 6/1/07	AOD480	TO-252	Single	General Purpose	N	No	No		30	20	10	10	60	30	28	42			3	710	72	7	2.7	5.8	15.6
AOD421	New		TO-252	Single	General Purpose	P	No	No		-20	12	-12.5	-8.9	18.8	8.4	75	95	145		-1.4	512	82	4.8	2.1	5.2	17
AOD422	Full Production		TO-252	Single	General Purpose	N	No	No		20	8	10	10	50	20		22	26	34	1	1160	146	18	3.6	6.2	51.7
AOD434	Last Time Buy 6/1/07		TO-252	Single	General Purpose	N	Yes	No		20	12	18	18	80	30	15	16	21	30	1	1810	200	17.9	4.7	2.5	49
AOD436	Last Time Buy 6/1/07		TO-252	Single	SMPS High Side	N	No	No		30	20	80	43	50	25	7.5	13			3	1520	214	18.2	9.6	7	24.2
AOD438	Last Time Buy 6/1/07		TO-252	Single	SMPS Low Side	N	No	No		30	20	85	83	100	50	3.5	5.5			3	3700	390	33	17.8	12	40
AOD442	Full Production		TO-252	Single	General Purpose	N	No	No		60	20	38	27	80	30	20	25			3	1920	116	24.2	14.4	7.4	28.2
AOD444	Full Production		TO-252	Single	General Purpose	N	No	No		60	20	12	12	20	10	60	85			3	450	22	3.8	1.9	4.2	16
AOD446	Full Production		TO-252	Single	General Purpose	N	No	No		75	25	10	10	20	10	140	165			3	293	20	*5.2	1.34	4.6	14.7
AOD448	Full Production		TO-252	Single	General Purpose	N	No	No		30	20	75	56	50	25	5	9			2.5	2342	320	26	13	9	30.7
AOD450	Full Production		TO-251	Single	Inverter	N	No	No		200	30	3.8	2.7	25	12.5	700				6	215	7.2	*3.82	1.47	8.3	10.5
AOD452	Full Production		TO-252	Single	SMPS High Side	N	No	No		25	20	55	55	50	25	8.5	14			3	1230	190	13.5	7.8	6.5	22.7
AOD454	Not for new designs	AOD488	TO-252	Single	General Purpose	N	No	No		40	20	12	12	50	25	33	47			3	404	37	4.5	2.6	3.5	13.2
AOD456	Full Production		TO-252	Single	SMPS Low Side	N	No	No		25	20	50	50	50	25	6	10			3	1850	225	15.7	8.2	7.5	30
AOD460	Not for new designs		TO-252	Single	SMPS	N	No	No		25	20	25	25	30	15	14	24			2.5	830	127	7.4	4.3	8	30
AOD464	Full Production		TO-252	Single	General Purpose	N	No	No		105	25	40	28	100	50	28				4	2038	85	*38.5	10	12.7	31.5
AOD466	Not for new designs	AOD484	TO-252	Single	SMPS	N	No	No		25	20	30	25	30	15	14	24			2.5	830	127	7.4	4.3	8	30
AOD472	Full Production		TO-252	Single	SMPS	N	No	No		25	20	50	50	50	25	6	9.5			2.5	2050	280	17	3.5	7.5	27
AOD476	Full Production		TO-252	Single	SMPS	N	No	No		20	16	25	23	33.3	16.7	21	28	78		2	900	105	7.2	2.8	4.5	18.7
AOD480	Full Production		TO-252	Single	General Purpose	N	No	No		30	20	25	21	33	17	23	36			2.5	621	85	5.7	3	4.5	15.1
AOD484	Full Production		TO-252	Single	SMPS	N	No	No		30	20	25	25	50	25	15	23			2.5	938	89	8.4	4.1	5	19
AOD486A	New		TO-252	Single	Inverter	N	No	No		40	20	50	36	50	25	9.8	13			3	1600	100	10.5	4.8	6.5	33
AOD488	Full Production		TO-252	Single	SMPS	N	No	No		40	20	20	15	20	10	26	39			3	404	37	4.5	2.6	3.5	13.2
AOD490	New		TO-252	Single	SMPS Low Side	N	No	Yes	SRFET	30	12	40	40	63	31	6.8	8.3			2.4	4000	217	27	11	9	37
AOD492	New		TO-252	Single	SMPS Low Side	N	No	Yes	SRFET	30	20	85	78	100	50	4.4	8.2			2.2	3260	314	29	12	8.5	3.4
AOD494	New		TO-252	Single	SMPS	N	No	No		30	12	55	39	63	31	11	13.5			2.5	1210	85	10	2.7	10	21
AOD496	New		TO-252	Single	SMPS	N	No	No		30	20	82	44	62.5	31	9.5	16			2.5	1000	340	18	4.8	5.6	18.5
AOD603	Full Production		TO-252-5L	Complementary	Inverter	N	No	No		80	20	12	12	2	1.3	60	85			3	450	27	3.8	1.9	4.2	16
						P	No	No		-60	20	-12	-10	2.5	1.6	115	150			-3	987	46	7.4	3.5	9	25
AOD604	Full Production		TO-252-5L	Complementary	Inverter	N	No	No		40	20	8	8	2	1.3	33	47			3	404	37	4.5	2.6	[illegible]	13.2

* Qg measured with VGS = 10V. In all other cases VGS = 4.5V.

ALPHA & OMEGA SEMICONDUCTOR

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Part Number	Status	Replacement Part	Package	Configuration	Popular Application	Type	ESD Diode	Schottky Diode	Schottky Type	V_{ds} (V)	V_{gs} (±V)	I_{DS} (A) 25°C	I_{DS} (A) 70°C	P_D (W) 25°C	P_D (W) 70°C	$R_{DS(ON)}$ (mΩ max) at V_{GS}= 10V	4.5V	2.5V	1.8V	VGS(th) (max V)	Ciss (pF)	Crss (pF)	Qg (nC)	Qgd (nC)	Td(on) (ns)	Td(off) (ns)
						P	No	No		-40	20	-8	-8	2.5	1.6	50	70			-3	657	83	14.1	4.1	8	24
AOD606	New		TO-252-4L	Complementary	Inverter	N	No	No		40	20	8	8	4.2	2.7	33	47			3	404	37	4.5	2.8	3.5	13.2
						P	No	No		-40	20	-8	-8	5	3.2	50	70			-3	657	63	7	4.1	8	24
AOD607	New		TO-252-4L	Complementary	Inverter	N	No	No		30	20	12		2.1	1.3	25	34			2.5	1040	110	9.8	3.5	4.5	17.4
						P	No	No		-30	20	-12		2.1	1.3	37	62			-2.4	920	122	9.7	5.4	9	20
AOD608	Full Production		TO-252-4L	Complementary	Inverter	N	Yes	No		40	20	10	10	2	1.3	39	50			3	500	38	4.1	2.6	4.8	17
						P	Yes	No		-40	20	-10	-10	2.5	1.6	51	75			-3	1000	77	8.8	4.5	9.7	35.5
AOL1401	New		Ultra SO8	Single	Battery Protection	P	Yes	No		-38	25	-19	-15	5	3	10				-3.5	3800	350	*61.2	15.4	13.5	97
AOL1408	Not for new designs	AOL1700	Ultra SO8	Single	SMPS Low Side	N	No	No		30	20	27	22	5	3	4	6			3	6060	355	46.4	15.6	15.7	55.5
AOL1412	New		Ultra SO8	Single	SMPS Low Side	N	No	Yes	SRFET	30	12	27	21	5	3	3.9	4.6			2.4	6430	352	44	13	17.5	56
AOL1414	Full Production		Ultra SO8	Single	SMPS High Side	N	No	No		30	12	21	17	5	3	6.5	7.5			2	2100	185	19.7	7.9	5.9	36.2
AOL1418	Full Production		Ultra SO8	Single	SMPS High Side	N	No	No		30	20	21	17	5	3	6.5	10.5			3	1320	154	13.3	6.6	7.2	22
AOL1420	Not for new designs	AOL1700	Ultra SO8	Single	SMPS Low Side	N	No	No		30	20	28	23	5	3	3.7	5.5			3	3700	390	33	17.6	12	40
AOL1424	New		Ultra SO8	Single	SMPS	N	Yes	No		30	20	24	19	5	3	5.4	8			2.5	2520	273	25.8	13.2	7	33
AOL1426	New		Ultra SO8	Single	SMPS High Side	N	No	No		30	12	15	12	4	2.6	10.5	13.5			2.5	1210	85	10	2.7	10	21
AOL1428	New		Ultra SO8	Single	SMPS High Side	N	No	No		30	20	18	14	5	3	9.5	16			2.5	1000	100	8.5	4.8	5.6	18.5
AOL1432	New		Ultra SO8	Single	SMPS High Side	N	No	No		25	20	21	17	6	4	8.5	14			3	1430	215	13.5	7.75	6.5	22.7
AOL1436	Not for new designs	AOL1428	Ultra SO8	Single	SMPS Low Side	N	No	No		25	30	20	16	5	3	11.5				4	1100	200	*17	6.8	9.5	11.5
AOL1440	New		Ultra SO8	Single	SMPS Low Side	N	No	No		25	30	25	20	5	3	5.2				4	2100	400	*33	14	12	15
AOL1444	Not for new designs	AOL1700	Ultra SO8	Single	SMPS Low Side	N	No	No		30	20	26	21	5	3	4.3	6.3			1	6070	375	46.4	15.8	15.7	55.5
AOL1446	Not for new designs	AOL1418	Ultra SO8	Single	SMPS High Side	N	No	No		30	20	21	16	5	3	7	11			3	1325	155	13.5	6.8	7.2	22
AOL1454	New		Ultra SO8	Single	Inverter	N	Yes	No		40	20	17	13	5	3.2	9	13			3	1600	100	10.5	4.8	6.5	33
AOL1700	New		Ultra SO8	Single	SMPS Low Side	N	No	Yes	SRFET	30	20	28	21	5	3.2	4.2	6			2.2	3760	314	29	12	9.5	34
AOL1702	New		Ultra SO8	Single	SMPS Low Side	N	No	Yes	SRFET	30	12	21	17	5	3.2	5.8	7.2			2.4	4000	217	27	11	9	37
AOL1704	New		Ultra SO8	Single	SMPS Low Side	N	No	Yes	SRFET	30	12	18	14	4.3	2.8	7.8	9.8			2.4	2800	145	18	6	7	31
AOL1708	New		Ultra SO8	Single	SMPS Low Side	N	No	Yes	SRFET	30	20	21	16.5	5	3.2	6.2	9.5			2	2154	185	17.8	7.6	8.8	25.2
AON3402	New		DFN 3x3	Single	General Purpose	N	Yes	No		20	12	12	9.6	3	1.9	13	17	26		1	1810	200	17.9	4.7	2.5	4.9
AON3408	New		DFN 3x3	Single	General Purpose	N	No	No		30	12	8.5	7.2	3	1.9	24	29	45		1.5	900	65	10	3.75	3.2	21.5
AON3601	Full Production		DFN 3x3	Complementary	Inverter	N	No	No		30	20	6.6	5.6	2	1.44	29	42			3	680	77	6.74	3.2	4.6	20.6
						P	No	No		-30	20	-5	-4.2	2	1.44	52	72			-3	700	75	7.6	3.8	8.3	29
AON3702	New		DFN 3x3	Single	SMPS Low Side	N	No	Yes	SRFET	30	12	11	8.8	3	1.9	14.5	18			1.8	1450	92	12	4.2	5.5	24
AON3806	New		DFN 3x3	Common Drain	Battery Protection	N	Yes	No		20	12	6.8	5.4	1.9	1.2		28	35		1	615	120	8.5	3	7	29
AON3810	New		DFN 3x3	Common Drain	Battery Protection	N	Yes	No		20	12	7	6	2.2	1.4	24	29	39	55	1	280	35	5.2	1.9	280	2350
AON3812	New		DFN 3x3	Common Drain	Battery Protection	N	Yes	No		30	12	6	5.3	2.2	1.4	27	30	40		1.5	330	10	6.4	2.5	388	2700
AON3814	New		DFN 3x3	Common Drain	Battery Protection	N	Yes	No		20	12	6	5.3	2.4	1.5		17	24	39	1.1	1315	183	13.1	4.6	1000	5600
AON3816	New		DFN 3x3	Common Drain	Battery Protection	N	Yes	No		20	12	4	4	2.4	1.5		22	28		1.1	1315	183	15	4.6	1000	5600
AON4413	New		DFN 2x3	Single	Load Switch	P	No	No		-30	20	4.7	3.7	1.6	1	46	60			2.5	688	92	12.7	4	7.7	20
AON4602	Not for new designs	AON4604	DFN 2x3	Complementary	Inverter	N	No	No		20	8	4.2	3.2	1.4	0.8		42	52	68	1	436	44	6.2	0.5	5.5	40
						P	No	No		-20	8	-3.4	-2.7	1.7	1.1		90	120	160	-1	540	49	6.1	1.6	10	44
AON4604	New		DFN 2x3	Complementary	Inverter	N	No	No		20	8	5.4	4.3	1.9	1.2		42	52	72	1	436	44	6.5	2.1	7	36.5
						P	No	No		-20	8	-3.8	-3	1.9	1.2		90	120	170	-1	540	49	5.9	1.9	11.5	37.5
AON4605	New		DFN 2x3	Complementary	Inverter	N	No	No		30	20	4.3	3.4	1.9	1.2	65	115			3	238	30	3.1	1.6	3.3	13.2
						P	No	No		-30	20	-3.4	-2.7	1.9	1.2	110	180			-3	290	44	3	1.6	7	15
AON4701	Not for new designs		DFN 2x3	Single	Load Switch	P	No	Yes	1A	-20	8	-3.4	-2.7	1.7	1.1		90	120	160	-1	540	49	6.1	1.6	10	44
AON4703	New		DFN 2x3	Single	Load Switch	P	No	Yes	1A	-20	8	-3.4	-2.7	1.7	1.1		90	120	160	-1	540	49	6.1	1.6	10	44
AON5800	Not for new designs		DFN 2x5	Common Drain	Battery Protection	N	Yes	No		20	12	8	6.3	1.6	1	16	20	27	45	1	1330	161	13.1	3.8	6.2	40.5
AON5802	Full Production		DFN 2x5	Common Drain	Battery Protection	N	Yes	No		30	12	7.2	5.6	1.7	1		20	30		1.5	1115	100	10.7	4.3	3.4	27.2
AON5808	Full Production		DFN 2x5	Common Drain	Battery Protection	N	Yes	No		20	12	7.2	5.8	1.7	1	20	23	32	50	1	615	120	8.5	3	7	29
AON5810	Full Production		DFN 2x5	Common Drain	Battery Protection	N	Yes	No		20	12	7.7	6.1	1.6	1		18	25	40	1	1360	178	13.1	3.9	6.2	40.5
AOP604	Not for new designs		PDIP-8	Complementary	Inverter	N	No	Yes	1A	30	20	7.5	6	2.5	1.6	28	43			3	680	77	6.74	3.2	4.6	20.6
						P	No	No		-30	20	-6.6	-5.3	2.5	1.6	35	58			-2.4	920	122	9.6	4.5	7.7	20.2
AOP605	Full Production		PDIP-8	Complementary	Inverter	N	No	No		30	20	7.5	6	2.5	1.6	28	43			3	680	77	6.74	3.2	4.6	20.6
						P	No	No		-30	20	-6.6	-5.3	2.5	1.6	35	58			-2.4	920	122	9.6	4.5	7.7	20.2
AOP606	Full Production		PDIP-8	Complementary	Inverter	N	No	No		60	20	7.9	6.3	3.1	2	25	30			3	1920	116	24.2	14.4	7.4	78.7
						P	No	No		-60	20	-6.1	-4.9	3.1	2	42	52			-2.4	2417	120	22.8	9.6	9.9	44
AOP607	Full Production		PDIP-8	Complementary	Inverter	N	N4	No		60	20	4.7	3.8	2.5	1.6	56	77			3	450	25	4.3	2.2	5.1	15.9
						P	No	No		-60	20	-3.4	-2.7	2.5	1.6	105	135			-3	930	35	8	3.2	8	31.5
AOP608	New		PDIP-8	Complementary	Inverter	N	No	No		40	20	6.3	5	2.5	1.6	33	46			3	404	37	4.6	7.5	4.3	15
						P	No	No		-40	20	-5.5	-4.4	2.5	1.6	45	63			-3	657	63	7.1	4.1	7.7	26.5
AOP609	New		PDIP-8	Complementary	Inverter	N	Yes	No		60	20	4.7	3.8	2.5	1.6	60	75			3	474	60	2.5	1.4	5.4	17.2
						P	Yes	No		-60	20	-3.5	-2.9	2.5	1.6	115	140			-3	897	36	3.9	1.7	9	35
AOP810	Full Production		PDIP-8	Complementary	Inverter	N	Yes	No	Yes	30	20	7.7	6.1	2.3	1.45	24	42			3	543	76	5.3	1.9	4.7	16.2
						P	Yes	No		-30	20	-6.2	-4.9	2.3	1.45	39	56			-3	1040	134	8.7	5	9	22.7
AOP611	New		PDIP-8	Complementary	Inverter	N	Yes	No		40	20	6.5	5.3	2.5	1.6	35	47			3	506	38	4.1	2.6	4.8	17
						P	Yes	No		-40	20	-5.5	-4.4	2.5	1.6	52	80			-3	1006	77	8.8	4.6	9.7	35.5
AOP800	Full Production		PDIP-8	Dual	General Purpose	N	No	No		30	20	9	7.3	2.5	1.6	20	28			3	940	119	9	4.7	5	19
AOP802	Full Production		PDIP-8	Dual	General Purpose	N	No	No		60	70	7.9	6.3	3.1	2	25	30			3	1920	116	24.2	14.4	7.4	28.2
AOP804	Full Production		PDIP-8	Dual	General Purpose	N	No	No		60	20	4.7	3.8	3.1	2	56	77			3	450	25	4.3	2.2	5.1	15.9
AOP806	Full Production		PDIP-8	Dual	General Purpose	N	No	No		75	25	3.4	2.7	2.5	1.6	132	168			3	290	24	*5.1	1.2	4	14.4
AOT400	Obsolete		TO-220	Single	SMPS Low Side	N	No	No		75	20	110	110	300	150	4.7				4	8390	450	167	45	29	80
AOT402	Obsolete		TO-220	Single	General Purpose	N	No	No		105	25	110	85	300	150	8.6				4	7700	300	*182	44	30.5	66
AOT404	Full Production		TO-220	Single	General Purpose	N	No	No		105	25	40	28	100	50	28				4	2038	85	*38.5	13.4	12.7	31.5
AOT424	Full Production		TO-220	Single	SMPS Low Side	N	No	No		30	20	110	88	100	50	4	5.5			3	3700	390	30.4	19.8	12.5	40
AOT426	Not for new designs		TO-220	Single	SMPS Low Side	N	No	No		30	20	85	82.5	75	37.5	6	11			2.5	2342	320	26	13	8	30.7
[illegible]	Full Production		TO-220	Single	General Purpose	N	No	No		75	30	80	57	115	58	11				4.5	3790	222	*65	23.5	[illegible]	30

* Qg measured with Vgs = 10V. In all other cases Vgs = 4.5V.

SEMICONDUCTOR

MOSFET Selector Guide

Part Number	Status	Replacement Part	Package	Configuration	Popular Application	Type	ESD Diode	Schottky Diode	Schottky Type	V_{DS} (V)	V_{GS} (±V)	I_D (A) 25°C	I_D (A) 70°C	P_D (W) 25°C	P_D (W) 70°C	$R_{DS(ON)}$ (mΩ max) at V_{GS}= 10V	4.5V	2.5V	1.8V	VGS(th) (max V)	Ciss (pF)	Crss (pF)	Qg (nC)	Qgd (nC)	Td(on) (ns)	Td(off) (ns)
AO3400	Not for new designs	AO3400A	SOT-23	Single	General Purpose	N	No	No		30	12	5.8	4.9	1.4	1	28	33	52		1.4	823	77	9.7	3.1	3.3	26.3
AO3400A	New		SOT-23	Single	General Purpose	N	No	No		30	12	5.7	4.7	1.4	0.9	26.5	32			1.5	900	65	10	3.75	3.2	21.5
AO3401	Not for new designs	AO3401A	SOT-23	Single	General Purpose	P	No	No		-30	12	-4.2	-3.5	1.4	1	50	65	120		-1.3	854	77	9.4	3	6.3	38.2
AO3401A	New		SOT-23	Single	General Purpose	P	No	No		-30	12	-4.3	-3.8	1.4	0.9	44	55	80		-1.3	933	81	9.3	3.7	5.2	42
AO3402	Full Production		SOT-23	Single	General Purpose	N	No	No		30	12	4	3.4	1.4	1	55	70	110		1.4	390	41	4.34	1.38	3.3	21.7
AO3403	Full Production		SOT-23	Single	General Purpose	P	No	No		-30	12	-2.6	-2.2	1.4	1	130	180	260		-1.4	409	42	4.4	1.32	5.3	31.5
AO3404	Not for new designs	AO3404A	SOT-23	Single	General Purpose	N	No	No		30	20	5.8	4.9	1.4	1	28	43			3	680	77	8.78	3.12	4.6	20.9
AO3404A	New		SOT-23	Single	General Purpose	N	No	No		30	20	5.8	4.9	1.4	0.9	28	42			3	621	85	5.7	3	4.5	15.1
AO3406	Full Production		SOT-23	Single	General Purpose	N	No	No		30	20	3.6	2.8	1.4	0.9	65	105			3	288	39	3.1	1.6	4.6	20.1
AO3407	Not for new designs	AO3407A	SOT-23	Single	General Purpose	P	No	No		-30	20	-4.1	-3.5	1.4	1	52	87			-3	700	75	7	3	8.6	28.2
AO3407A	New		SOT-23	Single	General Purpose	P	No	No		-30	20	-4.3	-3.5	1.4	0.9	48	78			-2.5	668	82	8.4	4	7.7	20
AO3409	Full Production		SOT-23	Single	General Purpose	P	No	No		-30	20	-2.6	-2.2	1.4	1	130	200			-3	302	37.8	2.4	0.95	7.5	17
AO3413	Full Production		SOT-23	Single	General Purpose	P	No	No		-20	8	-3	-2.4	1.4	0.9		87	130	190	-1	540	49	6.1	1.8	10	44
AO3414	Full Production		SOT-23	Single	General Purpose	N	No	No		20	8	4.2	3.2	1.4	0.9		50	63	87	1	436	44	8.2	0.5	5.5	40
AO3415	Full Production		SOT-23	Single	General Purpose	P	Yes	No		-20	8	-4	-3.5	1.4	0.9		43	54	73	-1	1450	160	17.2	4.5	9.5	94
AO3416	Full Production		SOT-23	Single	Load Switch	N	Yes	No		20	8	8.5	5.2	1.4	0.9		22	26	34	1	1160	146	16	3.6	6.2	51.7
AO3418	Full Production		SOT-23	Single	SMPS	N	No	No		30	12	3.8	3.1	1.4	0.9	60	70	155		1.8	226	29	3	0.65	2.6	14.5
AO3419	Full Production		SOT-23	Single	General Purpose	P	Yes	No		-20	12	-3.5	-2.8	1.4	0.9	75	85	145		-1.4	512	62	5.5	1.9	5	28
AO3420	Full Production		SOT-23	Single	Load Switch	N	No	No		20	12	6	5	1.4	0.9	24	27	42	55	1	630	137	8.8	3.7	5.5	29
AO3421	Full Production		SOT-23	Single	General Purpose	P	No	No		-30	20	-2.6	-2.2	1.4	1	130	200			-3	302	37.8	2.4	0.95	7.5	17
AO3422	Full Production		SOT-23	Single	General Purpose	N	No	No		55	12	2.1	1.7	1.25	0.8		160	200		2	214	12.6	2.6	0.8	2.3	16.5
AO3423	New		SOT-23	Single	General Purpose	P	No	No		-20	12	-2	-2	1.4	0.9	92	118	168		-1.4	512	62	5.5	19	5	28
AO3424	New		SOT-23	Single	General Purpose	N	No	No		30	12	2	2	1.4	0.9	80	95	157		1.8	226	28	2.6	0.5	2.6	14.5
AO3430	Full Production		SOT-23	Single	General Purpose	N	No	No		20	8	2	2	1.4	0.9	57	70	83		1	436	44	6.2	0.5	5.5	40
AO3434	New		SOT-23	Single	Battery Protection	N	Yes	No		30	20	3.5	2.8	1	0.64	52	75			1.8	269	41	3	0.65	2.6	15.2
AO3700	New		SOT-23-5	Single	General Purpose	N	Yes	No		30	12	3.3	2.6	1.16	0.7	65	75	160		2	226	29	4.6	0.55	2.6	14.5
AO3701	New		SOT-23-5	Single	General Purpose	P	Yes	No		-20	12	-3	-2.3	1.14	0.72	80	100	145		-1.4	512	62	5.5	1.9	5	28
AO3703	New		SOT-23-5	Single	General Purpose	P	No	YES	0.5A	-20	8	-2.7	-2.1	1.14	0.72		97	130	190	-1	540	49	6.1	1.8	10	44
AO4403	Full Production		SO-8	Single	General Purpose	P	No	No		-30	12	-6.1	-5.1	3	2.1	46	61	117		-1.3	940	73	9.4	3	7.6	44.7
AO4404	Not for new designs	AO4404B	SO-8	Single	General Purpose	N	No	No		30	12	8.5	7.1	3	2.1	24	30	48		1.4	857	71	9.7	3.1	3.3	26
AO4404B	New		SO-8	Single	General Purpose	N	No	No		30	12	8.5	7.1	2.8	1.8	24	30	48		1.5	900	65	10	3.75	3.3	21.5
AO4405	Not for new designs	AO4459	SO-8	Single	General Purpose	P	No	No		-30	20	-6	-5.1	3	2.1	50	85			-3	700	78	7.6	3.8	8.8	28.2
AO4406	Not for new designs		SO-8	Single	SMPS High Side	N	No	No		30	12	11.5	9.6	3	2.1	14	16.5	26		1.5	1630	142	18	5.5	4	32
AO4407	Full Production		SO-8	Single	Load Switch	P	No	No		-30	25	-12	-10	3	2.1	14				-3	2076	302	*37.2	10.4	12.4	25.6
AO4408	Not for new designs	AO4474	SO-8	Single	SMPS High Side	N	No	No		30	12	12	10	3	2.1	14	18.5			2.5	1020	80	10.3	3.9	3.8	19.2
AO4409	Full Production		SO-8	Single	Load Switch	P	No	No		-30	20	-15	-12.8	3	2.1	7.5	12			-2.7	5270	745	51.5	23	14	76.5
AO4410	Not for new designs	AO4706	SO-8	Single	SMPS Low Side	N	No	No		30	12	18	15	3	2.1	5.5	8.2			1.5	9130	387	72.4	16.8	11	99
AO4411	Not for new designs	AO4448	SO-8	Single	General Purpose	P	No	No		-30	20	-8	-6.6	3	2.1	33	55			-2.4	920	122	9.3	4.9	7.1	18.9
AO4412	Obsolete	AO4404B	SO-8	Single	SMPS High Side	N	No	No		30	12	8.5	7.1	3	2.1	26	34			3	590	40	6.04	2.58	3.7	14.9
AO4413	Full Production		SO-8	Single	Load Switch	P	No	No		-30	25	-15	-12.8	3	2.1	8.5				-3.5	4360	762	*78	23.6	17.5	49
AO4414	Last Time Buy 6/07/07	AO4466	SO-8	Single	General Purpose	N	No	No		30	20	8.5	7.1	3	2.1	26	40			3	680	77	6.74	3.32	4.5	20.1
AO4415	Full Production		SO-8	Single	Load Switch	P	No	No		-30	25	-8	-6.6	3	2.1	35				-3.5	893	151	*16.6	5.2	10.5	15.1
AO4418	Not for new designs	AO4466	SO-8	Single	General Purpose	N	No	No		30	25	11.5	9.7	3	2.1	17	40			3	758	128	*16.6	4.9	5.4	14.4
AO4419	Full Production		SO-8	Single	General Purpose	P	No	No		-30	20	-9.7	-8.1	3	2.1	20	35			-2.7	1573	211	13.7	8.8	9.5	44.2
AO4420	Not for new designs	AO4420A	SO-8	Single	General Purpose	N	No	No		30	12	13.7	9.7	3.1	2	10.5	12			2	3656	168	30.5	8.6	5.5	49.8
AO4420A	New		SO-8	Single	General Purpose	N	No	No		3d	12	13.7	9.7	3.1	2	10.5	12			2	3656	168	30.5	8.6	5.5	48.8
AO4421	Full Production		SO-8	Single	General Purpose	P	No	No		-60	20	-6.2	-5	3.1	2	40	50			-3	2417	120	22.7	9.2	9.8	44
AO4422	Lost Time Buy 6/07/07	AO4468	SO-8	Single	General Purpose	N	No	No		30	20	11	9.3	3	2.1	15	24			3	1040	110	9.8	3.5	4.5	17.4
AO4423	Full Production		SO-8	Single	Load Switch	P	Yes	No		-30	25	-15	-12.1	3.1	2	8.5				-3.5	4632	705	*82	23	18.5	55
AO4425	Full Production		SO-8	Single	Load Switch	P	Yes	No		-38	26	-14	-11	3.1	2	11				-3.5	3800	350	*63	18.1	12.4	97.5
AO4427	Full Production		SO-8	Single	Load Switch	P	Yes	No		-30	25	-12.5	-10.5	3	2.1	14				-3	2330	320	*41	12	12.8	48.5
AO4429	Not for new designs	AO4447	SO-8	Single	Load Switch	P	Yes	No		-30	20	-15	-12.8	3.1	2	7.7	12			-2.7	5355	620	46	21	15	82.5
AO4430	Full Production		SO-8	Single	General Purpose	N	No	No		30	20	18	15	3	2.1	5.5	7.5			2.5	6060	355	48	15	12	51.5
AO4433	New		SO-8	Single	Load Switch	P	Yes	No		-30	25	-11	-9.7	3	2.1	18				-3.5	1760	255	*30	8	11.5	35
AO4437	Full Production		SO-8	Single	Load Switch	P	Yes	No		-12	8	-11	-9	3	2.1		18	20	25	-1	3960	757	37	11	15	158
AO4438	Full Production		SO-8	Single	Display	N	No	No		60	20	8.2	6.6	3.1	2	22	27			3	1920	116	24.2	14.4	8.2	29.7
AO4440	Full Production		SO-8	Single	Display	N	No	No		60	20	5	4	2.5	1.6	55	75			2.5	450	25	4.3	2.2	5.1	15.9
AO4441	Full Production		SO-8	Single	Display	P	No	No		-60	20	-4	-3.1	3.1	2	100	130			-3	930	35	8	3.2	8	31.5
AO4442	Full Production		SO-8	Single	Display	N	No	No		75	25	3.1	2.5	2.5	1.6	130	165			3	303	17	*5.2	1.34	4.5	15.6
AO4443	Full Production		SO-8	Single	Display	P	No	No		-40	20	-6.5	-5	3.1	2	42	63			-3	657	63	7.1	4.1	7.7	26.5
AO4446	Not for new designs	AO4478	SO-8	Single	SMPS High Side	N	No	No		30	20	15	12	3	2.1	8.5	14.5			3	1520	214	17	10	7.2	22
AO4447	New		SO-8	Single	Load Switch	P	Yes	No		-30	20	-15	-13.6	3.1	2	7.5				-1.6	5500	473	45.2	19.4	12	100
AO4449	New		SO-8	Single	Load Switch	P	No	No		-30	20	-7	-4.6	3.1	2	34	54			-3	980	115	9.6	4.8	7.7	20
AO4450	Full Production		SO-8	Single	Display	N	No	No		40	20	6.6	5.2	2.5	1.6	30	43			3	404	37	4.6	2.5	4.3	15
AO4456	New		SO-8	Single	SMPS Low Side	N	No	Yes	SRFET	30	12	20	16	3.1	2	4.6	5.6			2.4	6430	352	44	13	17.5	56
AO4459	New		SO-8	Single	Load Switch	P	No	No		-30	20	-6.5	-5.3	3.1	2	46	72			-2.6	668	92	6.4	4	7.7	20
AO4466	New		SO-8	Single	SMPS High Side	N	No	No		30	20	9.4	7.7	3.1	2.1	23	35			3	621	85	5.7	3	4.5	15.1
AO4468	New		SO-8	Single	SMPS	N	No	No		30	20	11.6	9.2	3.1	2	14	22			3	955	112	9	4.7	5	19
AO4474	New		SO-8	Single	SMPS High Side	N	No	No		30	12	13.4	10.7	3.7	2.4	11.5	13.5			2.5	1210	330	22	2.7	10	21
AO4476	New		SO-8	Single	SMPS	N	No	No		30	20	15	12	3.7	2.4	10.5	17			2.5	1000	100	8.5	4.8	6	20
AO4480	Full Production		SO-8	single	Display	N	Yes	No		40	20	14	11	3.1	2	11.5	15.5			3	1600	100	10.5	4.8	3.5	13.2
AO4490	New		SO-8	single	Load Switch	N	Yes	No		30	20	16	13	2.8	1.8	7.2	10			2.5	1803	387	238	8.7	7.6	27
AO4600	Not for new designs	AO4622	SO-8	Complementary	Inverter	N	No	No		30	12	6.9	5.8	2	1.44	27	32	50		1.4	858	80	9.6	3	5.7	37
						P	No	No		-30	12	-5	-4.2	2	1.44	49	64	120		-1.4	952	77	9.5	3.1	12	37
AO4601	Full Production		SO-8	Complementary	Load Switch	N	No	No		30	12	4.7	4	2	1.44	55	70	110		1.4	390	41	0.6	4.34	3.3	21.7

Qg measured with Vgs = 10V. In all other cases Vgs = 4.5V.

ALPHA & OMEGA SEMICONDUCTOR

MOSFET Selector Guide - All Products

Part Number	Status	Replacement Part	Package	Configuration	Popular Application	Type	ESD Diode	Schottky Diode	Schottky Type	V_{DS} (V)	V_{GS} (±V)	I_{DS} (A)		P_D (W)		$R_{DS(ON)}$ (mΩ max) at V_{GS}=				VGS(th) (max V)	Ciss (pF)	Crss (pF)	Qg (nC)	Qgd (nC)	Td(on) (ns)	Td(off) (ns)
												25°C	70°C	25°C	70°C	10V	4.5V	2.5V	1.8V							
AOT430	Full Production		TO-220	Single	General Purpose	N	No	No		75	25	80	78	208	134	11.5				4	4700	180	*114	18	21	70
AOU400	Obsolete		TO-251	Single	General Purpose	N	No	No		60	20	38	27	60	30	20	25			3	1920	118	24.2	14.4	7.4	28.2
AOU401	Obsolete		TO-251	Single	General Purpose	P	No	No		-60	20	-26	-18	60	30	40	55			-2.4	2977	153	22.2	10	12	38
AOU402	Obsolete		TO-251	Single	General Purpose	N	No	No		60	20	12	8.5	20	10	60	85			3	385	20	3.8	1.9	4.2	16
AOU403	Obsolete		TO-251	Single	General Purpose	P	No	No		-60	20	-12	-10	50	25	115	150			-3	987	46	7.4	3.5	9	25
AOU404	Obsolete		TO-251	Single	General Purpose	N	No	No		75	25	10	10	20	10	140	165			3	293	20	*5.2	1.34	4.6	14.7
AOU405	Obsolete		TO-251	Single	General Purpose	P	No	No		-30	20	-18	-18	60	30	34	60			-2.4	920	122	8.7	6.4	9	20
AOU408	Obsolete		TO-220	Single	General Purpose	N	No	No		105	25	40	28	100	50	28				4	2038	85	*36.5	10	12.7	31.5
AOU412	Obsolete		TO-251	Single	SMPS High Side	N	No	No		30	20	85	65	100	50	7.5	11			2.5	1320	154	13.3	6.6	7.2	22
AOU413	Obsolete		TO-251	Single	General Purpose	P	No	No		-40	20	-12	-12	50	25	45	69			-3	657	63	7	4.1	8	24
AOU414	Obsolete		TO-251	Single	SMPS Low Side	N	No	No		30	20	85	73	100	50	5.7	7.5			2.4	6060	355	46.4	15.6	15.7	55.5
AOU417	Obsolete		TO-251	Single	Inverter	P	No	No		-30	20	-18	-18	50	25	22	40			-2.7	1573	211	15	7	11.7	42
AOU436	Obsolete		TO-251	Single	SMPS High Side	N	No	No		30	20	57	40	50	25	8.5	14			3	1520	214	16.2	9.6	7	24.2
AOU438	Obsolete		TO-251	Single	SMPS Low Side	N	No	No		30	20	85	83	100	50	4.5	6.5			3	3700	390	33	17.6	12	40
AOU452	Obsolete	AOI452	TO-251	Single	General Purpose	N	No	No		25	20	55	40	50	25	9	15			3	1230	180	13.5	7.75	6.5	22.7
AOU454	Obsolete		TO-251	Single	General Purpose	N	No	No		40	20	12	12	20	10	33	47			3	404	37	4.5	2.6	3.5	13.2
AOU456	Obsolete		TO-251	Single	General Purpose	N	No	No		25	20	50	50	50	25	7	10			3	1850	275	38	8.2	7.5	30
AOU460	Obsolete		TO-251	Single	SMPS	N	No	No		25	20	25	25	30	15	14	24			2.5	830	127	7.4	4.3	8	30
AOU472	Obsolete	AOI472	TO-251	Single	SMPS Low Side	N	No	No		25	20	50	50	50	25	6.7	10			2.5	2050	280	17	3.5	7.5	21

* Qg measured with Vgs = 10V. In all other cases Vgs = 4.5V.

EXHIBIT 2

EXHIBIT 2

INFRINGEMENT OF U.S. PATENT NO. 6,429,481

AOS AO4812 POWER MOSFET

CLAIM	AO4812 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AO4812 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AO4812-1 (datasheet); Fig. AO4812-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4812-1 (datasheet); Fig. AO4812-3 (Scanning Electron Microscopy image), item A; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending a predetermined depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. (Fig. AO4812-3 (Scanning Electron Microscopy image), item B; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AO4812-3 (Scanning Electron Microscopy image), item C; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AO4812-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well is less than the predetermined depth of the trench. (Fig. AO4812-3 (Scanning Electron Microscopy image), item D; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item D.)
a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,	The accused device has a highly doped heavy body formed with a higher concentration of P-type dopants (the second conductivity type) that is positioned adjacent to each source junction on the opposite side of the source junction from the trench. The P-type heavy body extends to a depth that is less than the depth of the well. (Fig. AO4812-3 (Scanning Electron Microscopy image), item E; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item E.)
wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The junction between the doped P-type heavy body and the well is an abrupt junction. (Fig. AO4812-5 (Secondary Ion Mass Spectroscopy data).) This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.

CLAIM	AO4812 POWER MOSFET
2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AO4812-3 (Scanning Electron Microscopy image), item D; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AO4812-3 (Scanning Electron Microscopy image), item B; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AO4812-5 (Secondary Ion Mass Spectroscopy data).)
18. The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate.	The accused device has an N-type epitaxial layer (formed with dopants of the first conductivity type) located between the N-type substrate and the lightly doped P-type well. (Fig. AO4812-3 (Scanning Electron Microscopy image), item F; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item F.) There is no indication of a buried layer formed at the interface between the epitaxial layer and the substrate.

61135796 v1

EXHIBIT 3

EXHIBIT 3

INFRINGEMENT OF U.S. PATENT NO. 6,429,481

AOS AO4468 POWER MOSFET

CLAIM	AO4468 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AO4468 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AO4468-1 (datasheet); Fig. AO4468-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4468-1 (datasheet); Fig. AO4468-3 (Scanning Electron Microscopy image), item A; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending a predetermined depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. (Fig. AO4468-3 (Scanning Electron Microscopy image), item B; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AO4468-3 (Scanning Electron Microscopy image), item C; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AO4468-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well is less than the predetermined depth of the trench. (Fig. AO4468-3 (Scanning Electron Microscopy image), item D; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item D.)
a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,	The accused device has a highly doped heavy body formed with a higher concentration of P-type dopants (the second conductivity type) that is positioned adjacent to each source junction on the opposite side of the source junction from the trench. The P-type heavy body extends to a depth that is less than the depth of the well. (Fig. AO4468-3 (Scanning Electron Microscopy image), item E; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item E.)
wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The junction between the doped P-type heavy body and the well is an abrupt junction. (Fig. AO4468-5 (Secondary Ion Mass Spectroscopy data).) This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.

CLAIM	AO4468 POWER MOSFET
2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AO4468-3 (Scanning Electron Microscopy image), item D; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AO4468-3 (Scanning Electron Microscopy image), item B; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AO4468-5 (Secondary Ion Mass Spectroscopy data).)
18. The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate.	The accused device has an N-type epitaxial layer (formed with dopants of the first conductivity type) located between the N-type substrate and the lightly doped P-type well. (Fig. AO4468-3 (Scanning Electron Microscopy image), item F; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item F.) There is no indication of a buried layer formed at the interface between the epitaxial layer and the substrate.

61138217 v1

EXHIBIT 4

EXHIBIT 4

INFRINGEMENT OF U.S. PATENT NO. 6,429,481

AOS AO6402 POWER MOSFET

CLAIM	AO6402 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AO6402 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AO6402-1 (datasheet); Fig. AO6402-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO6402-1 (datasheet); Fig. AO6402-3 (Scanning Electron Microscopy image), item A; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending a predetermined depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. (Fig. AO6402-3 (Scanning Electron Microscopy image), item B; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AO6402-3 (Scanning Electron Microscopy image), item C; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AO6402-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well is less than the predetermined depth of the trench. (Fig. AO6402-3 (Scanning Electron Microscopy image), item D; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item D.)
a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,	The accused device has a highly doped heavy body formed with a higher concentration of P-type dopants (the second conductivity type) that is positioned adjacent to each source junction on the opposite side of the source junction from the trench. The P-type heavy body extends to a depth that is less than the depth of the well. (Fig. AO6402-3 (Scanning Electron Microscopy image), item E; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item E.)
wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The junction between the doped P-type heavy body and the well is an abrupt junction. (Fig. AO6402-5 (Secondary Ion Mass Spectroscopy data).) This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.

CLAIM	AO6402 POWER MOSFET
2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AO6402-3 (Scanning Electron Microscopy image), item D; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AO6402-3 (Scanning Electron Microscopy image), item B; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AO6402-5 (Secondary Ion Mass Spectroscopy data).)
18. The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate.	The accused device has an N-type epitaxial layer (formed with dopants of the first conductivity type) located between the N-type substrate and the lightly doped P-type well. (Fig. AO6402-3 (Scanning Electron Microscopy image), item F; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item F.) There is no indication of a buried layer formed at the interface between the epitaxial layer and the substrate.

61138220 v1

EXHIBIT 5

EXHIBIT 5

INFRINGEMENT OF U.S. PATENT NO. 6,429,481

AOS AOL1412 POWER MOSFET

CLAIM	AOL1412 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AOL1412 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AOL1412-1 (datasheet); Fig. AOL1412-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AOL1412-1 (datasheet); Fig. AOL1412-3 (Scanning Electron Microscopy image), item A; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending a predetermined depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item B; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item C; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well is less than the predetermined depth of the trench. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item D; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item D.)
a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,	The accused device has a highly doped heavy body formed with a higher concentration of P-type dopants (the second conductivity type) that is positioned adjacent to each source junction on the opposite side of the source junction from the trench. The P-type heavy body extends to a depth that is less than the depth of the well. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item E; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item E.)
wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The junction between the doped P-type heavy body and the well is an abrupt junction. (Fig. AOL1412-5 (Secondary Ion Mass Spectroscopy data).) This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.

CLAIM	AOL1412 POWER MOSFET
2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item D; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item B; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AOL1412-5 (Secondary Ion Mass Spectroscopy data).)
18. The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate.	The accused device has an N-type epitaxial layer (formed with dopants of the first conductivity type) located between the N-type substrate and the lightly doped P-type well. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item F; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item F.) There is no indication of a buried layer formed at the interface between the epitaxial layer and the substrate.

61138244 v1

EXHIBIT 6

EXHIBIT 6

INFRINGEMENT OF U.S. PATENT NO. 6,429,481

AOS AO4410 POWER MOSFET

CLAIM	AO4410 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AO4410 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AO4410-1 (datasheet); Fig. AO4410-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4410-1 (datasheet); Fig. AO4410-3 (Scanning Electron Microscopy image), item A; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending a predetermined depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. (Fig. AO4410-3 (Scanning Electron Microscopy image), item B; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AO4410-3 (Scanning Electron Microscopy image), item C; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AO4410-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well is less than the predetermined depth of the trench. (Fig. AO4410-3 (Scanning Electron Microscopy image), item D; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item D.)
a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,	The accused device has a highly doped heavy body formed with a higher concentration of P-type dopants (the second conductivity type) that is positioned adjacent to each source junction on the opposite side of the source junction from the trench. The P-type heavy body extends to a depth that is less than the depth of the well. (Fig. AO4410-3 (Scanning Electron Microscopy image), item E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item E.)
wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The junction between the doped P-type heavy body and the well is an abrupt junction. (Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).) This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.

CLAIM	AO4410 POWER MOSFET
2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AO4410-3 (Scanning Electron Microscopy image), item D; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AO4410-3 (Scanning Electron Microscopy image), item B; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).)
18. The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate.	The accused device has an N-type epitaxial layer (formed with dopants of the first conductivity type) located between the N-type substrate and the lightly doped P-type well. (Fig. AO4410-3 (Scanning Electron Microscopy image), item F; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item F.) There is no indication of a buried layer formed at the interface between the epitaxial layer and the substrate.

61138253 v1

EXHIBIT 7

EXHIBIT 7

INFRINGEMENT OF U.S. PATENT NO. 6,429,481

AOS AO4914 POWER MOSFET

CLAIM	AO4914 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AO4914 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AO4914-1 (datasheet); Fig. AO4914-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4914-1 (datasheet); Fig. AO4914-3 (Scanning Electron Microscopy image), item A; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending a predetermined depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. (Fig. AO4914-3 (Scanning Electron Microscopy image), item B; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AO4914-3 (Scanning Electron Microscopy image), item C; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AO4914-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well is less than the predetermined depth of the trench. (Fig. AO4914-3 (Scanning Electron Microscopy image), item D; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item D.)
a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,	The accused device has a highly doped heavy body formed with a higher concentration of P-type dopants (the second conductivity type) that is positioned adjacent to each source junction on the opposite side of the source junction from the trench. The P-type heavy body extends to a depth that is less than the depth of the well. (Fig. AO4914-3 (Scanning Electron Microscopy image), item E; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item E.)
wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The junction between the doped P-type heavy body and the well is an abrupt junction. (Fig. AO4914-5 (Secondary Ion Mass Spectroscopy data).) This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.

CLAIM	AO4914 POWER MOSFET
2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AO4914-3 (Scanning Electron Microscopy image), item D; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AO4914-3 (Scanning Electron Microscopy image), item B; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AO4914-5 (Secondary Ion Mass Spectroscopy data).)
18. The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate.	The accused device has an N-type epitaxial layer (formed with dopants of the first conductivity type) located between the N-type substrate and the lightly doped P-type well. (Fig. AO4914-3 (Scanning Electron Microscopy image), item F; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item F.) There is no indication of a buried layer formed at the interface between the epitaxial layer and the substrate.

61138263 v1

EXHIBIT 8

EXHIBIT 8

INFRINGEMENT OF U.S. PATENT NO. 6,429,481

AOS AO4422 POWER MOSFET

CLAIM	AO4422 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AO4422 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AO4422-1 (datasheet); Fig. AO4422-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4422-1 (datasheet); Fig. AO4422-3 (Scanning Electron Microscopy image), item A; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending a predetermined depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. (Fig. AO4422-3 (Scanning Electron Microscopy image), item B; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AO4422-3 (Scanning Electron Microscopy image), item C; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AO4422-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well is less than the predetermined depth of the trench. (Fig. AO4422-3 (Scanning Electron Microscopy image), item D; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item D.)
a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,	The accused device has a highly doped heavy body formed with a higher concentration of P-type dopants (the second conductivity type) that is positioned adjacent to each source junction on the opposite side of the source junction from the trench. The P-type heavy body extends to a depth that is less than the depth of the well. (Fig. AO4422-3 (Scanning Electron Microscopy image), item E; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item E.)
wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The junction between the doped P-type heavy body and the well is an abrupt junction. (Fig. AO4422-5 (Secondary Ion Mass Spectroscopy data).) This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.

CLAIM	AO4422 POWER MOSFET
2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AO4422-3 (Scanning Electron Microscopy image), item D; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AO4422-3 (Scanning Electron Microscopy image), item B; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AO4422-5 (Secondary Ion Mass Spectroscopy data).)
18. The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate.	The accused device has an N-type epitaxial layer (formed with dopants of the first conductivity type) located between the N-type substrate and the lightly doped P-type well. (Fig. AO4422-3 (Scanning Electron Microscopy image), item F; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item F.) There is no indication of a buried layer formed at the interface between the epitaxial layer and the substrate.

61138269 v1

EXHIBIT 9

EXHIBIT 9

INFRINGEMENT OF U.S. PATENT NO. 6,429,481

AOS AO4704 POWER MOSFET

CLAIM	AO4704 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AO4704 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AO4704-1 (datasheet); Fig. AO4704-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4704-1 (datasheet); Fig. AO4704-3 (Scanning Electron Microscopy image), item A; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending a predetermined depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. (Fig. AO4704-3 (Scanning Electron Microscopy image), item B; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AO4704-3 (Scanning Electron Microscopy image), item C; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AO4704-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well is less than the predetermined depth of the trench. (Fig. AO4704-3 (Scanning Electron Microscopy image), item D; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item D.)
a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,	The accused device has a highly doped heavy body formed with a higher concentration of P-type dopants (the second conductivity type) that is positioned adjacent to each source junction on the opposite side of the source junction from the trench. The P-type heavy body extends to a depth that is less than the depth of the well. (Fig. AO4704-3 (Scanning Electron Microscopy image), item E; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item E.)
wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The junction between the doped P-type heavy body and the well is an abrupt junction. (Fig. AO4704-5 (Secondary Ion Mass Spectroscopy data).) This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.

CLAIM	AO4704 POWER MOSFET
2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AO4704-3 (Scanning Electron Microscopy image), item D; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AO4704-3 (Scanning Electron Microscopy image), item B; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AO4704-5 (Secondary Ion Mass Spectroscopy data).)
18. The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate.	The accused device has an N-type epitaxial layer (formed with dopants of the first conductivity type) located between the N-type substrate and the lightly doped P-type well. (Fig. AO4704-3 (Scanning Electron Microscopy image), item F; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item F.) There is no indication of a buried layer formed at the interface between the epitaxial layer and the substrate.

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EXHIBIT 10

EXHIBIT 10

INFRINGEMENT OF U.S. PATENT NO. 6,429,481

AOS AOD414 POWER MOSFET

CLAIM	AOD414 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AOD414 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AOD414-1 (datasheet); Fig. AOD414-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AOD414-1 (datasheet); Fig. AOD414-3 (Scanning Electron Microscopy image), item A; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending a predetermined depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. (Fig. AOD414-3 (Scanning Electron Microscopy image), item B; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AOD414-3 (Scanning Electron Microscopy image), item C; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AOD414-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well is less than the predetermined depth of the trench. (Fig. AOD414-3 (Scanning Electron Microscopy image), item D; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item D.)
a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,	The accused device has a highly doped heavy body formed with a higher concentration of P-type dopants (the second conductivity type) that is positioned adjacent to each source junction on the opposite side of the source junction from the trench. The P-type heavy body extends to a depth that is less than the depth of the well. (Fig. AOD414-3 (Scanning Electron Microscopy image), item E; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item E.)
wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The junction between the doped P-type heavy body and the well is an abrupt junction. (Fig. AOD414-5 (Secondary Ion Mass Spectroscopy data).) This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.

CLAIM	AOD414 POWER MOSFET
2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AOD414-3 (Scanning Electron Microscopy image), item D; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AOD414-3 (Scanning Electron Microscopy image), item B; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AOD414-5 (Secondary Ion Mass Spectroscopy data).)
18. The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate.	The accused device has an N-type epitaxial layer (formed with dopants of the first conductivity type) located between the N-type substrate and the lightly doped P-type well. (Fig. AOD414-3 (Scanning Electron Microscopy image), item F; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item F.) There is no indication of a buried layer formed at the interface between the epitaxial layer and the substrate.

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EXHIBIT 11

EXHIBIT 11

INFRINGEMENT OF U.S. PATENT NO. 6,429,481

AOS AO4413A POWER MOSFET

CLAIM	AO4413A POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AO4413A Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AO4413A-1 (datasheet); Fig. AO4413A-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is a P-channel MOSFET, which is therefore formed on a substrate of doped P-type silicon. In the language of the claim, the P-type dopants in the substrate are a "first conductivity type." (Fig. AO4413A-1 (datasheet); Fig. AO4413A-3 (Scanning Electron Microscopy image), item A; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending a predetermined depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item B; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item C; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is a P-channel MOSFET, the source junctions (regions) are formed with P-type dopants, which are dopants of the first conductivity type. (Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and	The accused device has a lightly doped well formed with N-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well is less than the predetermined depth of the trench. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item D; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item D.)
a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,	The accused device has a highly doped heavy body formed with a higher concentration of N-type dopants (the second conductivity type) that is positioned adjacent to each source junction on the opposite side of the source junction from the trench. The N-type heavy body extends to a depth that is less than the depth of the well. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item E; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item E.)
wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The junction between the doped N-type heavy body and the well is an abrupt junction. (Fig. AO4413A-5 (Secondary Ion Mass Spectroscopy data).) This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.

CLAIM	AO4413A POWER MOSFET
2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item D; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item B; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AO4413A-5 (Secondary Ion Mass Spectroscopy data).)
18. The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate.	The accused device has a P-type epitaxial layer (formed with dopants of the first conductivity type) located between the P-type substrate and the lightly doped N-type well. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item F; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item F.) There is no indication of a buried layer formed at the interface between the epitaxial layer and the substrate.

61138414 v1

EXHIBIT 12

EXHIBIT 12

INFRINGEMENT OF U.S. PATENT NO. 6,429,481

AOS AO6405 POWER MOSFET

CLAIM	AO6405 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AO6405 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AO6405-1 (datasheet); Fig. AO6405-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is a P-channel MOSFET, which is therefore formed on a substrate of doped P-type silicon. In the language of the claim, the P-type dopants in the substrate are a "first conductivity type." (Fig. AO6405-1 (datasheet); Fig. AO6405-3 (Scanning Electron Microscopy image), item A; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending a predetermined depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. (Fig. AO6405-3 (Scanning Electron Microscopy image), item B; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AO6405-3 (Scanning Electron Microscopy image), item C; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is a P-channel MOSFET, the source junctions (regions) are formed with P-type dopants, which are dopants of the first conductivity type. (Fig. AO6405-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and	The accused device has a lightly doped well formed with N-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well is less than the predetermined depth of the trench. (Fig. AO6405-3 (Scanning Electron Microscopy image), item D; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item D.)
a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,	The accused device has a highly doped heavy body formed with a higher concentration of N-type dopants (the second conductivity type) that is positioned adjacent to each source junction on the opposite side of the source junction from the trench. The N-type heavy body extends to a depth that is less than the depth of the well. (Fig. AO6405-3 (Scanning Electron Microscopy image), item E; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item E.)
wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The junction between the doped N-type heavy body and the well is an abrupt junction. (Fig. AO6405-5 (Secondary Ion Mass Spectroscopy data).) This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.

CLAIM	AO6405 POWER MOSFET
2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AO6405-3 (Scanning Electron Microscopy image), item D; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AO6405-3 (Scanning Electron Microscopy image), item B; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AO6405-5 (Secondary Ion Mass Spectroscopy data).)
18. The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate.	The accused device has a P-type epitaxial layer (formed with dopants of the first conductivity type) located between the P-type substrate and the lightly doped N-type well. (Fig. AO6405-3 (Scanning Electron Microscopy image), item F; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item F.) There is no indication of a buried layer formed at the interface between the epitaxial layer and the substrate.

61138412 v1

EXHIBIT 13

EXHIBIT 13

INFRINGEMENT OF U.S. PATENT NO. 6,429,481

AOS AO4912 POWER MOSFET

CLAIM	AO4912 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AO4912 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AO4912-1 (datasheet); Fig. AO4912-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4912-1 (datasheet); Fig. AO4912-3 (Scanning Electron Microscopy image), item A; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending a predetermined depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AO4912-3 (Scanning Electron Microscopy image), item C; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type.
a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well is less than the predetermined depth of the trench. (Fig. AO4912-3 (Scanning Electron Microscopy image), item D; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item D.)
a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,	The accused device has a highly doped heavy body formed with a higher concentration of P-type dopants (the second conductivity type) that is positioned adjacent to each source junction on the opposite side of the source junction from the trench. The P-type heavy body extends to a depth that is less than the depth of the well. (Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.)
wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The junction between the doped P-type heavy body and the well is an abrupt junction. (Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).) This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.

CLAIM	AO4912 POWER MOSFET
2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AO4912-3 (Scanning Electron Microscopy image), item D; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).)
6. An array of transistor cells comprising:	The accused device is formed with an array of transistor cells formed in a striped design as described below. (Fig. AO4912-3 (Scanning Electron Microscopy image); Fig. AO4912-4 (Scanning Capacitance Microscopy image); Fig. AO4912-6 (Scanning Electron Microscopy image (plan view).)
a semiconductor substrate having a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4912-1 (datasheet); Fig. AO4912-3 (Scanning Electron Microscopy image), item A; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item A.)
a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending a predetermined depth into said substrate and the space between adjacent trenches defining a contact area;	The accused device has gates formed using a striped design with substantially parallel trenches, with the trenches extending to a predetermined depth into the substrate and contact areas formed between the parallel trenches. (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B; Fig. AO4912-8 (Scanning Electron Microscopy image (plan view), items B and C.)
a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, the source junctions having the first conductivity type;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench and extending along the length of the trench. (Fig. AO4912-3 (Scanning Electron Microscopy image), item C; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item C; Fig. AO49124-8 (Scanning Electron Microscopy image (plan view), item A.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type.
a doped well having a second conductivity type with a charge opposite that of the first conductivity type, the doped well formed in the semiconductor substrate between each pair of gate-forming trenches;	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate between each pair of gate-forming trenches. (Fig. AO4912-3 (Scanning Electron Microscopy image), item D; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item D.)
a doped heavy body having the second conductivity type formed inside the doped well and positioned adjacent each source junction, the deepest portion of said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches; and	The accused device has a highly doped heavy body formed with a higher concentration of P-type dopants (the second conductivity type) that is formed inside the doped well and positioned adjacent to each source junction. The deepest portion of the P-type heavy body extends to a depth in the substrate that is less than the predetermined depth of the trenches. (Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.)

CLAIM	AO4912 POWER MOSFET
alternating heavy body and source contact regions defined at the surface of the semiconductor substrate along the length of the contact area,	The accused device has alternating doped heavy body and source contact regions at the surface of the substrate along the length of the contact area. (Fig. AO4912-9 (Scanning Capacitance Microscopy image), items B and C.)
wherein the heavy body forms an abrupt junction with the well, and a depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor.	The junction between the highly doped P-type heavy body and the lightly doped P-type well is an abrupt junction. (Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).) This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.
7. The array of transistor cells of claim 6, wherein each said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AO4912-3 (Scanning Electron Microscopy image), item D; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item D.)
8. The array of transistor cells of claim 6 wherein the controlled depth of the junction causes the breakdown origination point to occur approximately halfway between adjacent gate-forming trenches.	The depth of the abrupt junction is selected to cause the breakdown origination point to occur approximately halfway between adjacent gate-forming trenches. (Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).)
9. The array of transistor cells of claim 6 wherein each said doped well has a depth less than the predetermined depth of said gate-forming trenches.	The accused device has a doped well which has a depth that is less than the predetermined depth of the gate-forming trenches. (Fig. AO4912-3 (Scanning Electron Microscopy image), item D; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item D.)
10. The array of transistor cells of claim 6 wherein each said gate-forming trench has rounded top and bottom corners.	The trench of the accused device has rounded top and bottom corners. (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B.)
11. The array of transistor cells of claim 9 further comprising a field termination structure surrounding the periphery of the array.	The accused device has a field termination structure surrounding the periphery of the array. (Fig. AO4912-6 (Scanning Electron Microscopy image), item A.)
15. A trenched field effect transistor formed on a substrate, comprising:	The accused device is a trenched field effect transistor formed on a substrate. (Fig. AO4912-1 (datasheet); Fig. AO4912-3 (Scanning Electron Microscopy image), item A; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item A.)
a plurality of trenches formed in parallel along a longitudinal axis, the plurality of trenches extending into the substrate to a first depth;	The accused device has a plurality of trenches formed in parallel along a longitudinal axis, the trenches extending to a first depth into the substrate. (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B; Fig. AO4912-6 (Scanning Electron Microscopy image (plan view), item B.)
a doped well extending into the substrate between each pair of trenches;	The accused device has a doped well formed in the substrate between each pair of trenches. (Fig. AO4912-3 (Scanning Electron Microscopy image), item D; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item D.)

CLAIM	AO4912 POWER MOSFET
a pair of doped source regions formed on opposite sides of each trench; and	The accused device has a pair of doped source regions formed on opposite sides of each trench. (Fig. AO4912-3 (Scanning Electron Microscopy image), item C; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item C.) Since the accused device is an N-channel device, the source regions are doped with N-type dopants.
a doped heavy body formed inside the doped well adjacent each source region, the doped heavy body extending into the doped well to a second depth that is less than the first depth,	The accused device has a doped heavy body formed with a higher concentration of P-type dopants than is located inside the doped well. The doped heavy body extends to a second depth that is less than the first depth of the trench. (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.)
wherein the doped heavy body:	
forms a continuous doped region along substantially the entire longitudinal axis of a trench, and	The doped heavy body forms a continuous region along substantially the entire longitudinal axis of the trench. (Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.)
forms an abrupt junction with the well, and a depth of the heavy body junction relative to a maximum depth of the well, is adjusted so that a peak electric field in the substrate is spaced away from the trench when voltage is applied to the transistor.	The junction between the highly doped P-type heavy body and the lightly doped P-type well is an abrupt junction. (Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).) This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.
16. The trenched field effect transistor of claim 15 further comprising source and heavy body contact areas defined on a surface of the substrate between each pair of trenches.	The accused device has source and heavy body contact areas at the surface of the substrate between each pair of trenches. (Fig. AO4912-9 (Scanning Capacitance Microscopy image (plan view)).)
17. The trenched field effect transistor of claim 16 wherein the contact areas alternate between source and heavy body contacts.	The source and heavy body contact areas alternate at the surface of the substrate between each pair of trenches. (Fig. AO4912-9 (Scanning Capacitance Microscopy image (plan view)).)
18. The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate.	The accused device has an N-type epitaxial layer (formed with dopants of the first conductivity type) located between the N-type substrate and the lightly doped P-type well. (Fig. AO4912-3 (Scanning Electron Microscopy image), items A, D, F; Fig. AO4912-4 (Scanning Capacitance Microscopy image), items A, D, F.) There is no indication of a buried layer formed at the interface between the epitaxial layer and the substrate.
21. The trenched field effect transistor of claim 6, further comprising:	
an epitaxial layer having the first conductivity type formed between the substrate and the well, with no buried layer formed at an interface between the epitaxial layer and the substrate.	The accused device has an N-type epitaxial layer (formed with dopants of the first conductivity type) located between the N-type substrate and the lightly doped P-type well. (Fig. AO4912-3 (Scanning Electron Microscopy image), items A, D, F; Fig. AO4912-4 (Scanning Capacitance Microscopy image), items A, D, F.) There is no indication of a buried layer formed at the interface between the epitaxial layer and the substrate.

CLAIM	AO4912 POWER MOSFET
22. The trenched field effect transistor of claim 15, further comprising:	
an epitaxial layer having the first conductivity type formed between the substrate and the well,	The accused device has an N-type epitaxial layer (formed with dopants of the first conductivity type) located between the N-type substrate and the lightly doped P-type well. (Fig. AO4912-3 (Scanning Electron Microscopy image), items A, D, F; Fig. AO4912-4 (Scanning Capacitance Microscopy image), items A, D, F.)
wherein the second depth relative to a depth of the well is adjusted to eliminate the need for any layers disposed between the epitaxial layer and the substrate.	The accused device has a doped heavy body formed at depth relative to the depth of the P-type well such that there is no need for any layers disposed between the epitaxial layer and the substrate. (Fig. AO4912-3 (Scanning Electron Microscopy image), items D and E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), items D and E.)

61139165 v1

EXHIBIT 14

EXHIBIT 14

INFRINGEMENT OF U.S. PATENT NO. 6,429,481

AOS AOD438 POWER MOSFET

CLAIM	AOD438 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AOD438 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AOD438-1 (datasheet); Fig. AOD438-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AOD438-1 (datasheet); Fig. AOD438-3 (Scanning Electron Microscopy image), item A; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending a predetermined depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AOD438-3 (Scanning Electron Microscopy image), item C; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type.
a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well is less than the predetermined depth of the trench. (Fig. AOD438-3 (Scanning Electron Microscopy image), item D; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item D.)
a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,	The accused device has a highly doped heavy body formed with a higher concentration of P-type dopants (the second conductivity type) that is positioned adjacent to each source junction on the opposite side of the source junction from the trench. The P-type heavy body extends to a depth that is less than the depth of the well. (Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.)
wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The junction between the doped P-type heavy body and the well is an abrupt junction. (Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).) This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.

CLAIM	AOD438 POWER MOSFET
2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AOD438-3 (Scanning Electron Microscopy image), item D; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).)
6. An array of transistor cells comprising:	The accused device is formed with an array of transistor cells formed in a striped design as described below. (Fig. AOD438-3 (Scanning Electron Microscopy image); Fig. AOD438-4 (Scanning Capacitance Microscopy image); Fig. AOD438-6 (Scanning Electron Microscopy image (plan view).)
a semiconductor substrate having a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AOD438-1 (datasheet); Fig. AOD438-3 (Scanning Electron Microscopy image), item A; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item A.)
a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending a predetermined depth into said substrate and the space between adjacent trenches defining a contact area;	The accused device has gates formed using a striped design with substantially parallel trenches, with the trenches extending to a predetermined depth into the substrate and contact areas formed between the parallel trenches. (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B; Fig. AOD438-8 (Scanning Electron Microscopy image (plan view), items B and C.)
a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, the source junctions having the first conductivity type;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench and extending along the length of the trench. (Fig. AOD438-3 (Scanning Electron Microscopy image), item C; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item C; Fig. AOD4384-8 (Scanning Electron Microscopy image (plan view), item A.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type.
a doped well having a second conductivity type with a charge opposite that of the first conductivity type, the doped well formed in the semiconductor substrate between each pair of gate-forming trenches;	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate between each pair of gate-forming trenches. (Fig. AOD438-3 (Scanning Electron Microscopy image), item D; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item D.)
a doped heavy body having the second conductivity type formed inside the doped well and positioned adjacent each source junction, the deepest portion of said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches; and	The accused device has a highly doped heavy body formed with a higher concentration of P-type dopants (the second conductivity type) that is formed inside the doped well and positioned adjacent to each source junction. The deepest portion of the P-type heavy body extends to a depth in the substrate that is less than the predetermined depth of the trenches. (Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.)

CLAIM	AOD438 POWER MOSFET
alternating heavy body and source contact regions defined at the surface of the semiconductor substrate along the length of the contact area,	The accused device has alternating doped heavy body and source contact regions at the surface of the substrate along the length of the contact area. (Fig. AOD438-9 (Scanning Capacitance Microscopy image), items B and C.)
wherein the heavy body forms an abrupt junction with the well, and a depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor.	The junction between the highly doped P-type heavy body and the lightly doped P-type well is an abrupt junction. (Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).) This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.
7. The array of transistor cells of claim 6, wherein each said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AOD438-3 (Scanning Electron Microscopy image), item D; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item D.)
8. The array of transistor cells of claim 6 wherein the controlled depth of the junction causes the breakdown origination point to occur approximately halfway between adjacent gate-forming trenches.	The depth of the abrupt junction is selected to cause the breakdown origination point to occur approximately halfway between adjacent gate-forming trenches. (Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).)
9. The array of transistor cells of claim 6 wherein each said doped well has a depth less than the predetermined depth of said gate-forming trenches.	The accused device has a doped well which has a depth that is less than the predetermined depth of the gate-forming trenches. (Fig. AOD438-3 (Scanning Electron Microscopy image), item D; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item D.)
10. The array of transistor cells of claim 6 wherein each said gate-forming trench has rounded top and bottom corners.	The trench of the accused device has rounded top and bottom corners. (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B.)
11. The array of transistor cells of claim 9 further comprising a field termination structure surrounding the periphery of the array.	The accused device has a field termination structure surrounding the periphery of the array. (Fig. AOD438-6 (Scanning Electron Microscopy image), item A.)
15. A trenched field effect transistor formed on a substrate, comprising:	The accused device is a trenched field effect transistor formed on a substrate. (Fig. AOD438-1 (datasheet); Fig. AOD438-3 (Scanning Electron Microscopy image), item A; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item A.)
a plurality of trenches formed in parallel along a longitudinal axis, the plurality of trenches extending into the substrate to a first depth;	The accused device has a plurality of trenches formed in parallel along a longitudinal axis, the trenches extending to a first depth into the substrate. (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B; Fig. AOD438-6 (Scanning Electron Microscopy image (plan view), item B.)
a doped well extending into the substrate between each pair of trenches;	The accused device has a doped well formed in the substrate between each pair of trenches. (Fig. AOD438-3 (Scanning Electron Microscopy image), item D; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item D.)

CLAIM	AOD438 POWER MOSFET
a pair of doped source regions formed on opposite sides of each trench; and	The accused device has a pair of doped source regions formed on opposite sides of each trench. (Fig. AOD438-3 (Scanning Electron Microscopy image), item C; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item C.) Since the accused device is an N-channel device, the source regions are doped with N-type dopants.
a doped heavy body formed inside the doped well adjacent each source region, the doped heavy body extending into the doped well to a second depth that is less than the first depth,	The accused device has a doped heavy body formed with a higher concentration of P-type dopants than is located inside the doped well. The doped heavy body extends to a second depth that is less than the first depth of the trench. (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.)
wherein the doped heavy body:	
forms a continuous doped region along substantially the entire longitudinal axis of a trench, and	The doped heavy body forms a continuous region along substantially the entire longitudinal axis of the trench. (Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.)
forms an abrupt junction with the well, and a depth of the heavy body junction relative to a maximum depth of the well, is adjusted so that a peak electric field in the substrate is spaced away from the trench when voltage is applied to the transistor.	The junction between the highly doped P-type heavy body and the lightly doped P-type well is an abrupt junction. (Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).) This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.
16. The trenched field effect transistor of claim 15 further comprising source and heavy body contact areas defined on a surface of the substrate between each pair of trenches.	The accused device has source and heavy body contact areas at the surface of the substrate between each pair of trenches. (Fig. AOD438-9 (Scanning Capacitance Microscopy image (plan view)).)
17. The trenched field effect transistor of claim 16 wherein the contact areas alternate between source and heavy body contacts.	The source and heavy body contact areas alternate at the surface of the substrate between each pair of trenches. (Fig. AOD438-9 (Scanning Capacitance Microscopy image (plan view)).)
18. The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate.	The accused device has an N-type epitaxial layer (formed with dopants of the first conductivity type) located between the N-type substrate and the lightly doped P-type well. (Fig. AOD438-3 (Scanning Electron Microscopy image), items A, D, F; Fig. AOD438-4 (Scanning Capacitance Microscopy image), items A, D, F.) There is no indication of a buried layer formed at the interface between the epitaxial layer and the substrate.
21. The trenched field effect transistor of claim 6, further comprising:	
an epitaxial layer having the first conductivity type formed between the substrate and the well, with no buried layer formed at an interface between the epitaxial layer and the substrate.	The accused device has an N-type epitaxial layer (formed with dopants of the first conductivity type) located between the N-type substrate and the lightly doped P-type well. (Fig. AOD438-3 (Scanning Electron Microscopy image), items A, D, F; Fig. AOD438-4 (Scanning Capacitance Microscopy image), items A, D, F.) There is no indication of a buried layer formed at the interface between the epitaxial layer and the substrate.

CLAIM	AOD438 POWER MOSFET
22. The trenched field effect transistor of claim 15, further comprising:	
an epitaxial layer having the first conductivity type formed between the substrate and the well,	The accused device has an N-type epitaxial layer (formed with dopants of the first conductivity type) located between the N-type substrate and the lightly doped P-type well. (Fig. AOD438-3 (Scanning Electron Microscopy image), items A, D, F; Fig. AOD438-4 (Scanning Capacitance Microscopy image), items A, D, F.)
wherein the second depth relative to a depth of the well is adjusted to eliminate the need for any layers disposed between the epitaxial layer and the substrate.	The accused device has a doped heavy body formed at depth relative to the depth of the P-type well such that there is no need for any layers disposed between the epitaxial layer and the substrate. (Fig. AOD438-3 (Scanning Electron Microscopy image), items D and E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), items D and E.)

61139184 v1

EXHIBIT 15

EXHIBIT 15

INFRINGEMENT OF U.S. PATENT NO. 6,429,481

AOS AOL1414 POWER MOSFET

CLAIM	AOL1414 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AOL1414 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AOL1414-1 (datasheet); Fig. AOL1414-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AOL1414-1 (datasheet); Fig. AOL1414-3 (Scanning Electron Microscopy image), item A; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending a predetermined depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item C; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type.
a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well is less than the predetermined depth of the trench. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item D; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item D.)
a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,	The accused device has a highly doped heavy body formed with a higher concentration of P-type dopants (the second conductivity type) that is positioned adjacent to each source junction on the opposite side of the source junction from the trench. The P-type heavy body extends to a depth that is less than the depth of the well. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.)
wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The junction between the doped P-type heavy body and the well is an abrupt junction. (Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).) This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.

CLAIM	AOL1414 POWER MOSFET
2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item D; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).)
6. An array of transistor cells comprising:	The accused device is formed with an array of transistor cells formed in a striped design as described below. (Fig. AOL1414-3 (Scanning Electron Microscopy image); Fig. AOL1414-4 (Scanning Capacitance Microscopy image); Fig. AOL1414-6 (Scanning Electron Microscopy image (plan view).)
a semiconductor substrate having a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AOL1414-1 (datasheet); Fig. AOL1414-3 (Scanning Electron Microscopy image), item A; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item A.)
a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending a predetermined depth into said substrate and the space between adjacent trenches defining a contact area;	The accused device has gates formed using a striped design with substantially parallel trenches, with the trenches extending to a predetermined depth into the substrate and contact areas formed between the parallel trenches. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B; Fig. AOL1414-8 (Scanning Electron Microscopy image (plan view), items B and C.)
a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, the source junctions having the first conductivity type;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench and extending along the length of the trench. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item C; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item C; Fig. AOL1414-8 (Scanning Electron Microscopy image (plan view), item A.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type.
a doped well having a second conductivity type with a charge opposite that of the first conductivity type, the doped well formed in the semiconductor substrate between each pair of gate-forming trenches;	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate between each pair of gate-forming trenches. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item D; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item D.)
a doped heavy body having the second conductivity type formed inside the doped well and positioned adjacent each source junction, the deepest portion of said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches; and	The accused device has a highly doped heavy body formed with a higher concentration of P-type dopants (the second conductivity type) that is formed inside the doped well and positioned adjacent to each source junction. The deepest portion of the P-type heavy body extends to a depth in the substrate that is less than the predetermined depth of the trenches. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.)

CLAIM	AOL1414 POWER MOSFET
alternating heavy body and source contact regions defined at the surface of the semiconductor substrate along the length of the contact area,	The accused device has alternating doped heavy body and source contact regions at the surface of the substrate along the length of the contact area. (Fig. AOL1414-9 (Scanning Capacitance Microscopy image), items B and C.)
wherein the heavy body forms an abrupt junction with the well, and a depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor.	The junction between the highly doped P-type heavy body and the lightly doped P-type well is an abrupt junction. (Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).) This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.
7. The array of transistor cells of claim 6, wherein each said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item D; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item D.)
8. The array of transistor cells of claim 6 wherein the controlled depth of the junction causes the breakdown origination point to occur approximately halfway between adjacent gate-forming trenches.	The depth of the abrupt junction in the accused device is selected to cause the breakdown origination point to occur approximately halfway between adjacent gate-forming trenches. (Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).)
9. The array of transistor cells of claim 6 wherein each said doped well has a depth less than the predetermined depth of said gate-forming trenches.	The accused device has a doped well which has a depth that is less than the predetermined depth of the gate-forming trenches. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item D; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item D.)
10. The array of transistor cells of claim 6 wherein each said gate-forming trench has rounded top and bottom corners.	The trench of the accused device has rounded top and bottom corners. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B.)
11. The array of transistor cells of claim 9 further comprising a field termination structure surrounding the periphery of the array.	The accused device has a field termination structure surrounding the periphery of the array. (Fig. AOL1414-6 (Scanning Electron Microscopy image), item A.)
15. A trenched field effect transistor formed on a substrate, comprising:	The accused device is a trenched field effect transistor formed on a substrate. (Fig. AOL1414-1 (datasheet); Fig. AOL1414-3 (Scanning Electron Microscopy image), item A; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item A.)
a plurality of trenches formed in parallel along a longitudinal axis, the plurality of trenches extending into the substrate to a first depth;	The accused device has a plurality of trenches formed in parallel along a longitudinal axis, the trenches extending to a first depth into the substrate. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B; Fig. AOL1414-6 (Scanning Electron Microscopy image (plan view), item B.)
a doped well extending into the substrate between each pair of trenches;	The accused device has a doped well formed in the substrate between each pair of trenches. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item D; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item D.)

CLAIM	AOL1414 POWER MOSFET
a pair of doped source regions formed on opposite sides of each trench; and	The accused device has a pair of doped source regions formed on opposite sides of each trench. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item C; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item C.) Since the accused device is an N-channel device, the source regions are doped with N-type dopants.
a doped heavy body formed inside the doped well adjacent each source region, the doped heavy body extending into the doped well to a second depth that is less than the first depth,	The accused device has a doped heavy body formed with a higher concentration of P-type dopants than is located inside the doped well. The doped heavy body extends to a second depth that is less than the first depth of the trench. (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.)
wherein the doped heavy body:	
forms a continuous doped region along substantially the entire longitudinal axis of a trench, and	The doped heavy body forms a continuous region along substantially the entire longitudinal axis of the trench. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.)
forms an abrupt junction with the well, and a depth of the heavy body junction relative to a maximum depth of the well, is adjusted so that a peak electric field in the substrate is spaced away from the trench when voltage is applied to the transistor.	The junction between the highly doped P-type heavy body and the lightly doped P-type well is an abrupt junction. (Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).) This abrupt junction creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.
16. The trenched field effect transistor of claim 15 further comprising source and heavy body contact areas defined on a surface of the substrate between each pair of trenches.	The accused device has source and heavy body contact areas at the surface of the substrate between each pair of trenches. (Fig. AOL1414-9 (Scanning Capacitance Microscopy image (plan view)).)
17. The trenched field effect transistor of claim 16 wherein the contact areas alternate between source and heavy body contacts.	The source and heavy body contact areas alternate at the surface of the substrate between each pair of trenches. (Fig. AOL1414-9 (Scanning Capacitance Microscopy image (plan view)).)
18. The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate.	The accused device has an N-type epitaxial layer (formed with dopants of the first conductivity type) located between the N-type substrate and the lightly doped P-type well. (Fig. AOL1414-3 (Scanning Electron Microscopy image), items A, D, F; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), items A, D, F.) There is no indication of a buried layer formed at the interface between the epitaxial layer and the substrate.
21. The trenched field effect transistor of claim 6, further comprising:	
an epitaxial layer having the first conductivity type formed between the substrate and the well, with no buried layer formed at an interface between the epitaxial layer and the substrate.	The accused device has an N-type epitaxial layer (formed with dopants of the first conductivity type) located between the N-type substrate and the lightly doped P-type well. (Fig. AOL1414-3 (Scanning Electron Microscopy image), items A, D, F; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), items A, D, F.) There is no indication of a buried layer formed at the interface between the epitaxial layer and the substrate.

CLAIM	AOL1414 POWER MOSFET
22. The trenched field effect transistor of claim 15, further comprising:	
an epitaxial layer having the first conductivity type formed between the substrate and the well,	The accused device has an N-type epitaxial layer (formed with dopants of the first conductivity type) located between the N-type substrate and the lightly doped P-type well. (Fig. AOL1414-3 (Scanning Electron Microscopy image), items A, D, F; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), items A, D, F.)
wherein the second depth relative to a depth of the well is adjusted to eliminate the need for any layers disposed between the epitaxial layer and the substrate.	The accused device has a doped heavy body formed at depth relative to the depth of the P-type well such that there is no need for any layers disposed between the epitaxial layer and the substrate. (Fig. AOL1414-3 (Scanning Electron Microscopy image), items D and E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), items D and E.)

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EXHIBIT 16

EXHIBIT 16

INFRINGEMENT OF U.S. PATENT NO. 6,710,406 B2

AOS AO4812 POWER MOSFET

CLAIM	AO4812 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AO4812 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AO4812-1 (datasheet); Fig. AO4812-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4812-1 (datasheet); Fig. AO4812-3 (Scanning Electron Microscopy image), item A; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending to a first depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. In the language of the claim, the predetermined depth to which the trench extends is a "first depth." (Fig. AO4812-3 (Scanning Electron Microscopy image), item B; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AO4812-3 (Scanning Electron Microscopy image), item C; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AO4812-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type, and formed into the substrate to a second depth that is less than said first depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well (a second depth) is less than the predetermined depth of the trench (a first depth). (Fig. AO4812-3 (Scanning Electron Microscopy image), item D; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item D.)
a heavy body formed in said doped well extending to a third depth that is less than said second depth of said doped well, the heavy body forming an abrupt junction with the well;	The accused device has a heavy body formed in the doped well that extends to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AO4812-3 (Scanning Electron Microscopy image), item E; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item E.) The junction between the doped P-type heavy body and the doped well is an abrupt junction. (Fig. AO4812-5 (Secondary Ion Mass Spectroscopy data).)
wherein, a location of the abrupt junction relative to the depth of the well is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The location of the abrupt junction of the accused device is such that it creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench. (Fig. AO4812-5 (Secondary Ion Mass Spectroscopy data).)
2. The trenched field effect transistor of claim 1	The accused device has a doped well with a substantially flat bottom. (Fig.

CLAIM	AO4812 POWER MOSFET
wherein said doped well has a substantially flat bottom.	AO4812-3 (Scanning Electron Microscopy image), item D; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AO4812-3 (Scanning Electron Microscopy image), item B; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AO4812-5 (Secondary Ion Mass Spectroscopy data).)
5. The trenched field effect transistor of claim 1 wherein the heavy body comprises a heavily doped region having dopants of the second conductivity type at the abrupt junction.	The heavy body of the accused device is a heavily doped region of P-type dopants (a second conductivity type). (Fig. AO4812-3 (Scanning Electron Microscopy image), item E; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item E.)
6. The trenched field effect transistor of claim 5 wherein the heavily doped region is formed by implanting dopants of the second conductivity type at approximately the third depth.	The heavy body of the accused device is formed by implanting P-type dopants (a second conductivity type) in the doped well and extending to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AO4812-3 (Scanning Electron Microscopy image), item E; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item E.)
10. The trenched field effect transistor of claim 1 wherein the trench is lined with a dielectric layer and substantially filled with conductive material.	The trench of the accused device is lined with a dielectric layer and substantially filled with doped polysilicon (a conductive material). (Fig. AO4812-3 (Scanning Electron Microscopy image), items B and G; Fig. AO4812-4 (Scanning Capacitance Microscopy image), items B and G.)
11. The trenched field effect transistor of claim 10 wherein the conductive material comprises polysilicon.	The conductive material in the trench of the accused device is doped polysilicon. (Fig. AO4812-3 (Scanning Electron Microscopy image), item B; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item B.)
12. The trenched field effect transistor of claim 10 wherein the conductive material filling the trench is recessed relative to the surface of the semiconductor substrate.	The conductive polysilicon filling the trench of the accused device is recessed relative to the surface of the silicon semiconductor substrate. (Fig. AO4812-3 (Scanning Electron Microscopy image), item B; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item B.)

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EXHIBIT 17

EXHIBIT 17

INFRINGEMENT OF U.S. PATENT NO. 6,710,406 B2

AOS AO4468 POWER MOSFET

CLAIM	AO4468 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AO4468 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AO4468-1 (datasheet); Fig. AO4468-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4468-1 (datasheet); Fig. AO4468-3 (Scanning Electron Microscopy image), item A; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending to a first depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. In the language of the claim, the predetermined depth to which the trench extends is a "first depth." (Fig. AO4468-3 (Scanning Electron Microscopy image), item B; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AO4468-3 (Scanning Electron Microscopy image), item C; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AO4468-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type, and formed into the substrate to a second depth that is less than said first depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well (a second depth) is less than the predetermined depth of the trench (a first depth). (Fig. AO4468-3 (Scanning Electron Microscopy image), item D; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item D.)
a heavy body formed in said doped well extending to a third depth that is less than said second depth of said doped well, the heavy body forming an abrupt junction with the well;	The accused device has a heavy body formed in the doped well that extends to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AO4468-3 (Scanning Electron Microscopy image), item E; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item E.) The junction between the doped P-type heavy body and the doped well is an abrupt junction. (Fig. AO4468-5 (Secondary Ion Mass Spectroscopy data).)
wherein, a location of the abrupt junction relative to the depth of the well is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The location of the abrupt junction of the accused device is such that it creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench. (Fig. AO4468-5 (Secondary Ion Mass Spectroscopy data).)
2. The trenched field effect transistor of claim 1	The accused device has a doped well with a substantially flat bottom. (Fig.

CLAIM	AO4468 POWER MOSFET
wherein said doped well has a substantially flat bottom.	AO4468-3 (Scanning Electron Microscopy image), item D; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AO4468-3 (Scanning Electron Microscopy image), item B; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AO4468-5 (Secondary Ion Mass Spectroscopy data).)
5. The trenched field effect transistor of claim 1 wherein the heavy body comprises a heavily doped region having dopants of the second conductivity type at the abrupt junction.	The heavy body of the accused device is a heavily doped region of P-type dopants (a second conductivity type). (Fig. AO4468-3 (Scanning Electron Microscopy image), item E; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item E.)
6. The trenched field effect transistor of claim 5 wherein the heavily doped region is formed by implanting dopants of the second conductivity type at approximately the third depth.	The heavy body of the accused device is formed by implanting P-type dopants (a second conductivity type) in the doped well and extending to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AO4468-3 (Scanning Electron Microscopy image), item E; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item E.)
10. The trenched field effect transistor of claim 1 wherein the trench is lined with a dielectric layer and substantially filled with conductive material.	The trench of the accused device is lined with a dielectric layer and substantially filled with doped polysilicon (a conductive material). (Fig. AO4468-3 (Scanning Electron Microscopy image), items B and G; Fig. AO4468-4 (Scanning Capacitance Microscopy image), items B and G.)
11. The trenched field effect transistor of claim 10 wherein the conductive material comprises polysilicon.	The conductive material in the trench of the accused device is doped polysilicon. (Fig. AO4468-3 (Scanning Electron Microscopy image), item B; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item B.)
12. The trenched field effect transistor of claim 10 wherein the conductive material filling the trench is recessed relative to the surface of the semiconductor substrate.	The conductive polysilicon filling the trench of the accused device is recessed relative to the surface of the silicon semiconductor substrate. (Fig. AO4468-3 (Scanning Electron Microscopy image), item B; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item B.)

EXHIBIT 18

EXHIBIT 18

INFRINGEMENT OF U.S. PATENT NO. 6,710,406 B2

AOS AO6402 POWER MOSFET

CLAIM	AO6402 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AO6402 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AO6402-1 (datasheet); Fig. AO6402-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO6402-1 (datasheet); Fig. AO6402-3 (Scanning Electron Microscopy image), item A; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending to a first depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. In the language of the claim, the predetermined depth to which the trench extends is a "first depth." (Fig. AO6402-3 (Scanning Electron Microscopy image), item B; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AO6402-3 (Scanning Electron Microscopy image), item C; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AO6402-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type, and formed into the substrate to a second depth that is less than said first depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well (a second depth) is less than the predetermined depth of the trench (a first depth). (Fig. AO6402-3 (Scanning Electron Microscopy image), item D; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item D.)
a heavy body formed in said doped well extending to a third depth that is less than said second depth of said doped well, the heavy body forming an abrupt junction with the well;	The accused device has a heavy body formed in the doped well that extends to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AO6402-3 (Scanning Electron Microscopy image), item E; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item E.) The junction between the doped P-type heavy body and the doped well is an abrupt junction. (Fig. AO6402-5 (Secondary Ion Mass Spectroscopy data).)
wherein, a location of the abrupt junction relative to the depth of the well is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The location of the abrupt junction of the accused device is such that it creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench. (Fig. AO6402-5 (Secondary Ion Mass Spectroscopy data).)
2. The trenched field effect transistor of claim 1	The accused device has a doped well with a substantially flat bottom. (Fig.

CLAIM	AO6402 POWER MOSFET
wherein said doped well has a substantially flat bottom.	AO6402-3 (Scanning Electron Microscopy image), item D; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AO6402-3 (Scanning Electron Microscopy image), item B; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AO6402-5 (Secondary Ion Mass Spectroscopy data).)
5. The trenched field effect transistor of claim 1 wherein the heavy body comprises a heavily doped region having dopants of the second conductivity type at the abrupt junction.	The heavy body of the accused device is a heavily doped region of P-type dopants (a second conductivity type). (Fig. AO6402-3 (Scanning Electron Microscopy image), item E; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item E.)
6. The trenched field effect transistor of claim 5 wherein the heavily doped region is formed by implanting dopants of the second conductivity type at approximately the third depth.	The heavy body of the accused device is formed by implanting P-type dopants (a second conductivity type) in the doped well and extending to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AO6402-3 (Scanning Electron Microscopy image), item E; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item E.)
10. The trenched field effect transistor of claim 1 wherein the trench is lined with a dielectric layer and substantially filled with conductive material.	The trench of the accused device is lined with a dielectric layer and substantially filled with doped polysilicon (a conductive material). (Fig. AO6402-3 (Scanning Electron Microscopy image), items B and G; Fig. AO6402-4 (Scanning Capacitance Microscopy image), items B and G.)
11. The trenched field effect transistor of claim 10 wherein the conductive material comprises polysilicon.	The conductive material in the trench of the accused device is doped polysilicon. (Fig. AO6402-3 (Scanning Electron Microscopy image), item B; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item B.)
12. The trenched field effect transistor of claim 10 wherein the conductive material filling the trench is recessed relative to the surface of the semiconductor substrate.	The conductive polysilicon filling the trench of the accused device is recessed relative to the surface of the silicon semiconductor substrate. (Fig. AO6402-3 (Scanning Electron Microscopy image), item B; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item B.)

EXHIBIT 19

EXHIBIT 19

INFRINGEMENT OF U.S. PATENT NO. 6,710,406 B2

AOS AOL1412 POWER MOSFET

CLAIM	AOL1412 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AOL1412 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AOL1412-1 (datasheet); Fig. AOL1412-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AOL1412-1 (datasheet); Fig. AOL1412-3 (Scanning Electron Microscopy image), item A; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending to a first depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. In the language of the claim, the predetermined depth to which the trench extends is a "first depth." (Fig. AOL1412-3 (Scanning Electron Microscopy image), item B; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item C; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type, and formed into the substrate to a second depth that is less than said first depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well (a second depth) is less than the predetermined depth of the trench (a first depth). (Fig. AOL1412-3 (Scanning Electron Microscopy image), item D; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item D.)
a heavy body formed in said doped well extending to a third depth that is less than said second depth of said doped well, the heavy body forming an abrupt junction with the well;	The accused device has a heavy body formed in the doped well that extends to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AOL1412-3 (Scanning Electron Microscopy image), item E; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item E.) The junction between the doped P-type heavy body and the doped well is an abrupt junction. (Fig. AOL1412-5 (Secondary Ion Mass Spectroscopy data).)
wherein, a location of the abrupt junction relative to the depth of the well is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The location of the abrupt junction of the accused device is such that it creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench. (Fig. AOL1412-5 (Secondary Ion Mass Spectroscopy data).)
2. The trenched field effect transistor of claim 1	The accused device has a doped well with a substantially flat bottom. (Fig.

CLAIM	AOL1412 POWER MOSFET
wherein said doped well has a substantially flat bottom.	AOL1412-3 (Scanning Electron Microscopy image), item D; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item B; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AOL1412-5 (Secondary Ion Mass Spectroscopy data).)
5. The trenched field effect transistor of claim 1 wherein the heavy body comprises a heavily doped region having dopants of the second conductivity type at the abrupt junction.	The heavy body of the accused device is a heavily doped region of P-type dopants (a second conductivity type). (Fig. AOL1412-3 (Scanning Electron Microscopy image), item E; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item E.)
6. The trenched field effect transistor of claim 5 wherein the heavily doped region is formed by implanting dopants of the second conductivity type at approximately the third depth.	The heavy body of the accused device is formed by implanting P-type dopants (a second conductivity type) in the doped well and extending to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AOL1412-3 (Scanning Electron Microscopy image), item E; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item E.)
10. The trenched field effect transistor of claim 1 wherein the trench is lined with a dielectric layer and substantially filled with conductive material.	The trench of the accused device is lined with a dielectric layer and substantially filled with doped polysilicon (a conductive material). (Fig. AOL1412-3 (Scanning Electron Microscopy image), items B and G; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), items B and G.)
11. The trenched field effect transistor of claim 10 wherein the conductive material comprises polysilicon.	The conductive material in the trench of the accused device is doped polysilicon. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item B; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item B.)
12. The trenched field effect transistor of claim 10 wherein the conductive material filling the trench is recessed relative to the surface of the semiconductor substrate.	The conductive polysilicon filling the trench of the accused device is recessed relative to the surface of the silicon semiconductor substrate. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item B; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item B.)